

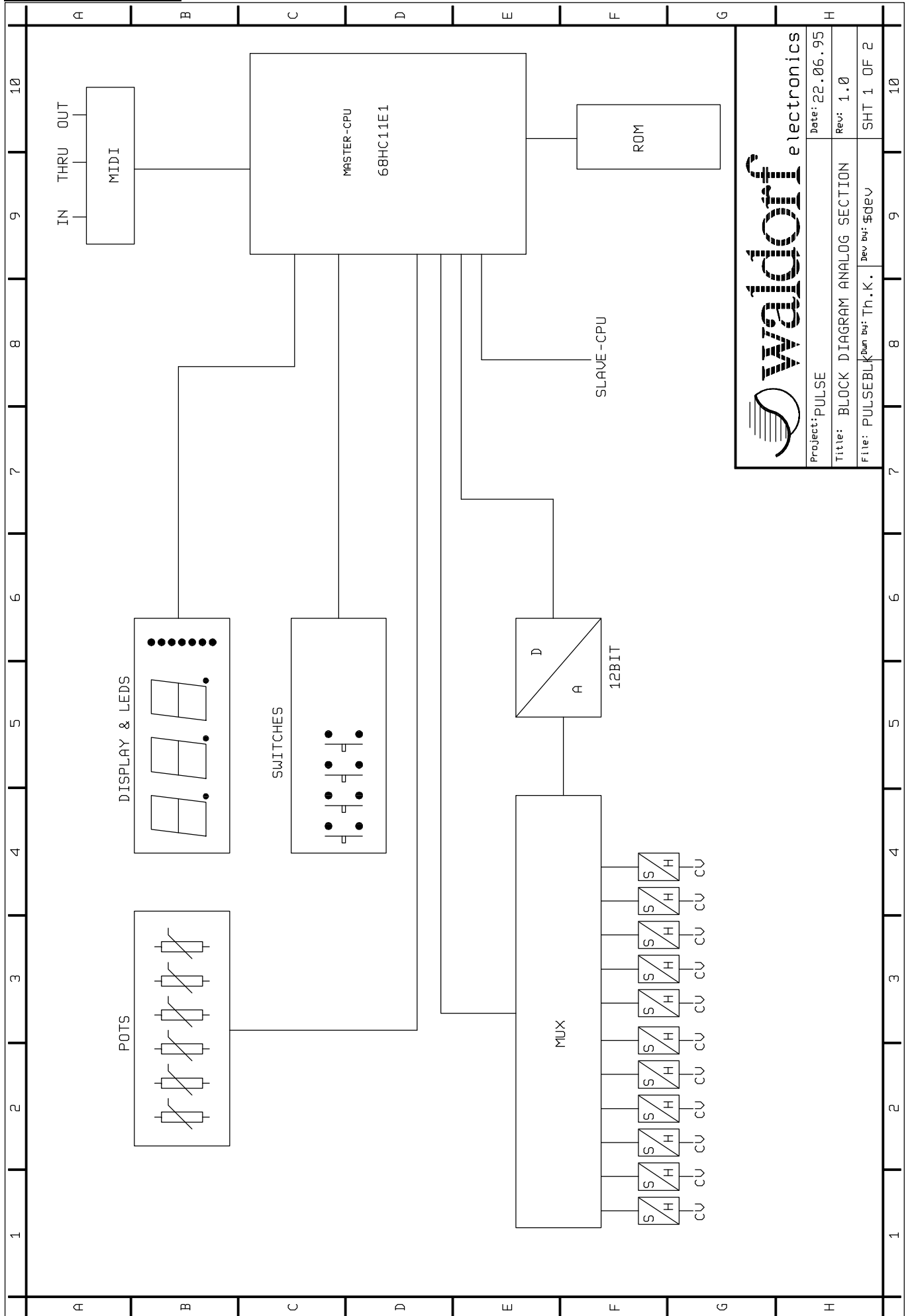
# DOKUMENTATION

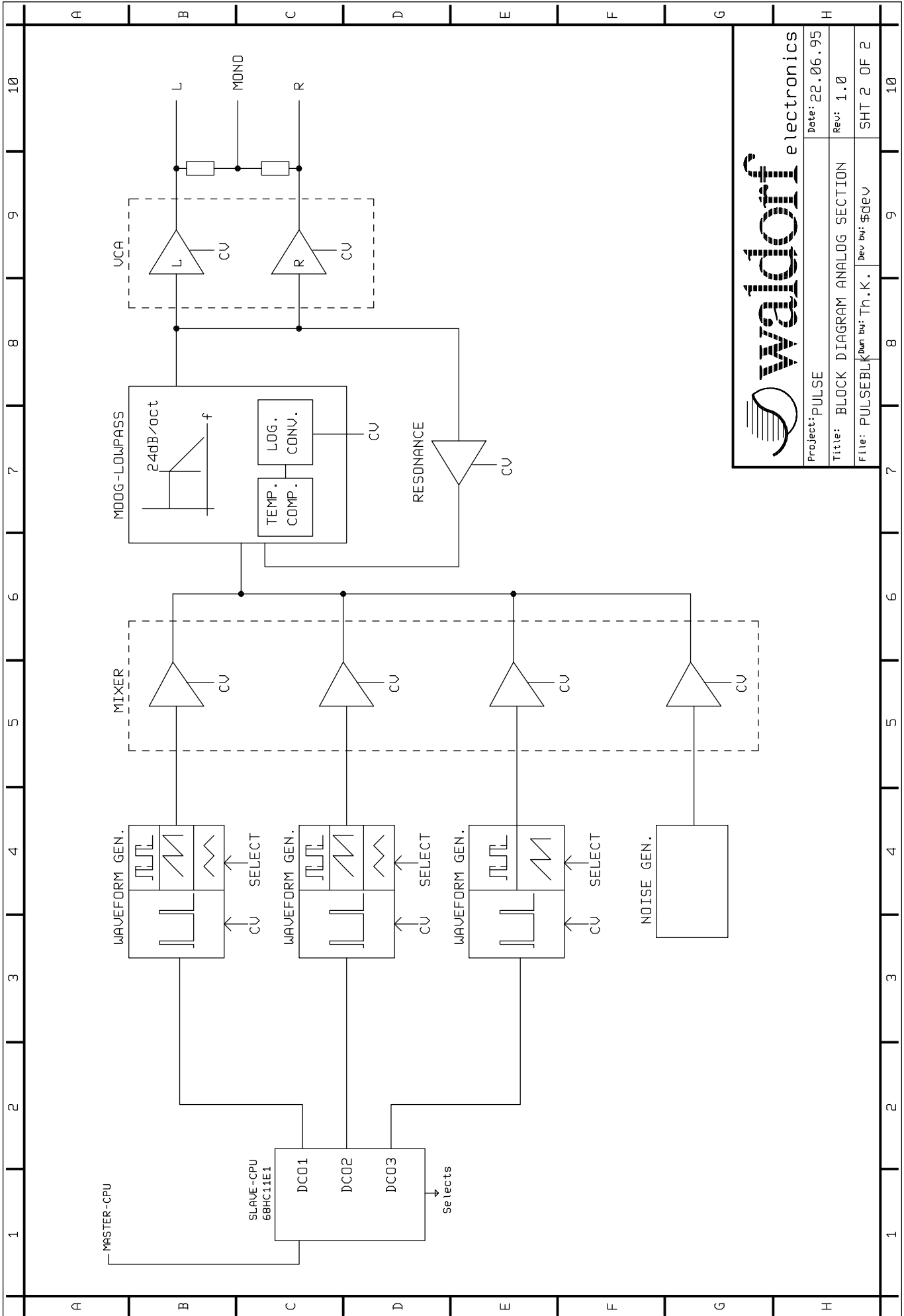
## PULSE

Stand: 01.11.95 , Rev.: 3.1



# Blockschaltbilder

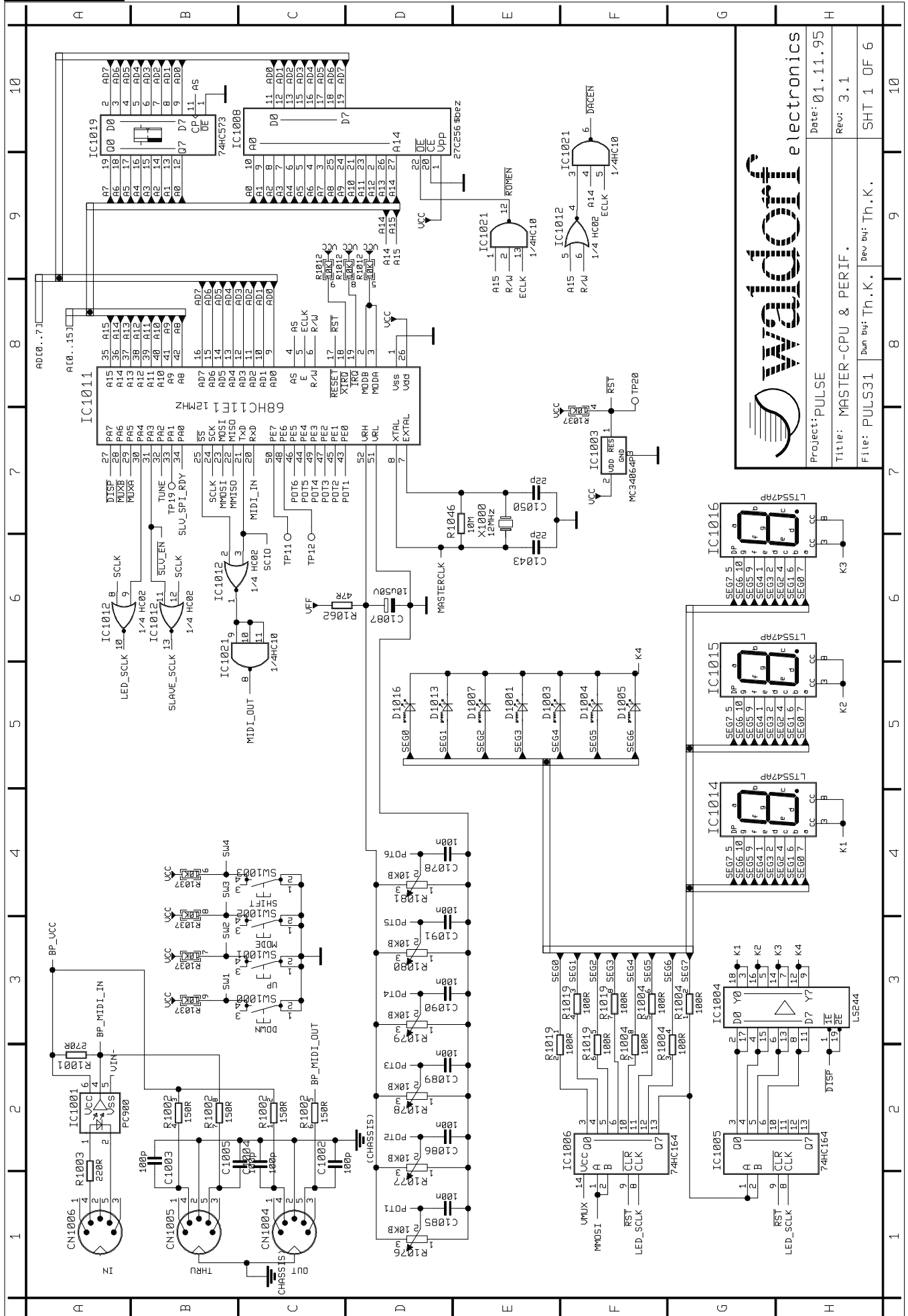




**waldoff** electronics

Project: PULS31  
 Date: 22.06.95  
 Title: BLOCK DIAGRAM ANALOG SECTION  
 Rev: 1.0  
 File: PULSEBL.dwg  
 Rev by: \$dev  
 SHT 2 OF 2

# Schaltpläne

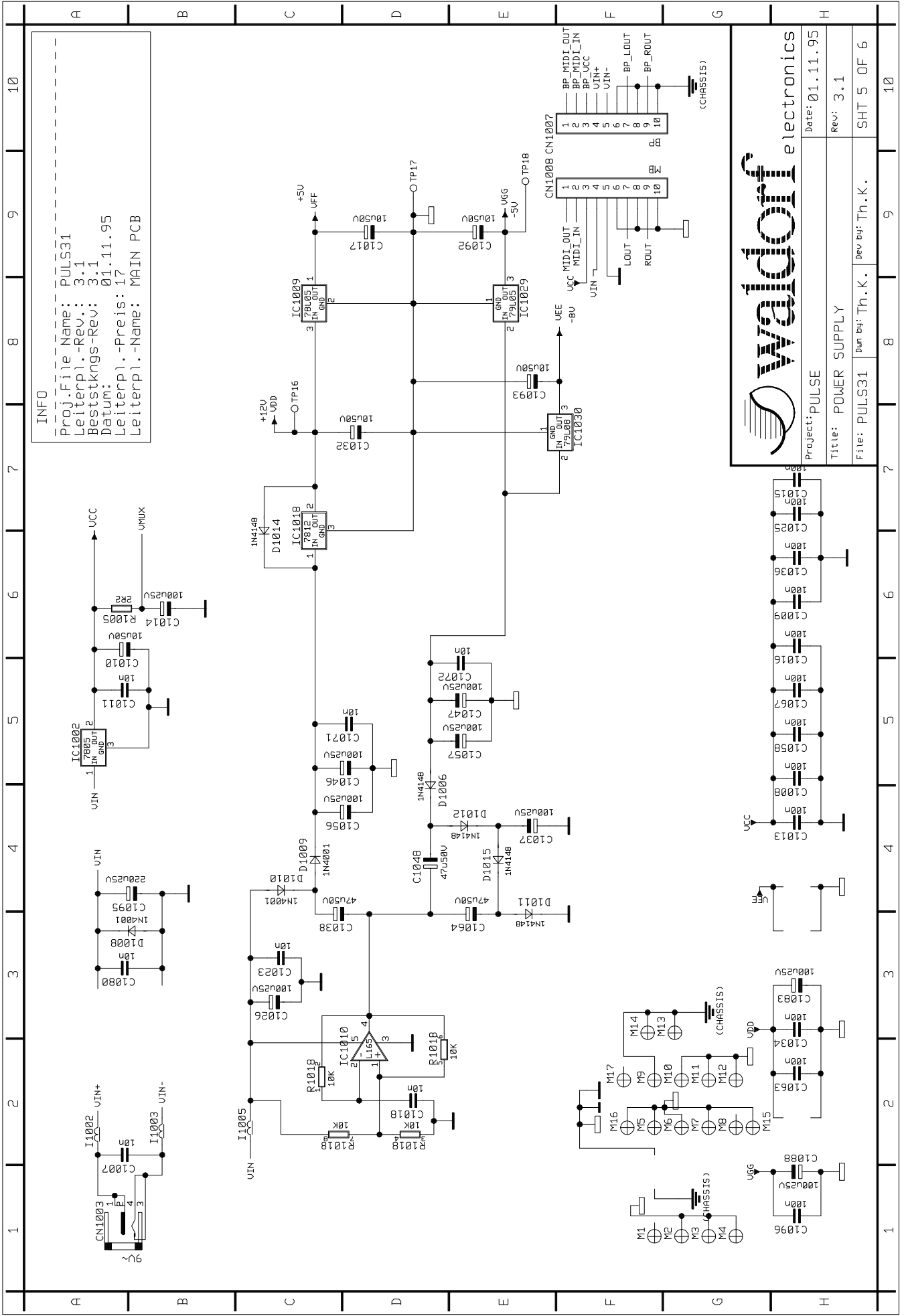


Project: PULSE  
 Title: MASTER-CPU & PERIF.  
 Date: 01.11.95  
 Rev: 3.1  
 File: PULS31  
 Dev by: Th.K.  
 Sum by: Th.K.  
 SHT 1 OF 6





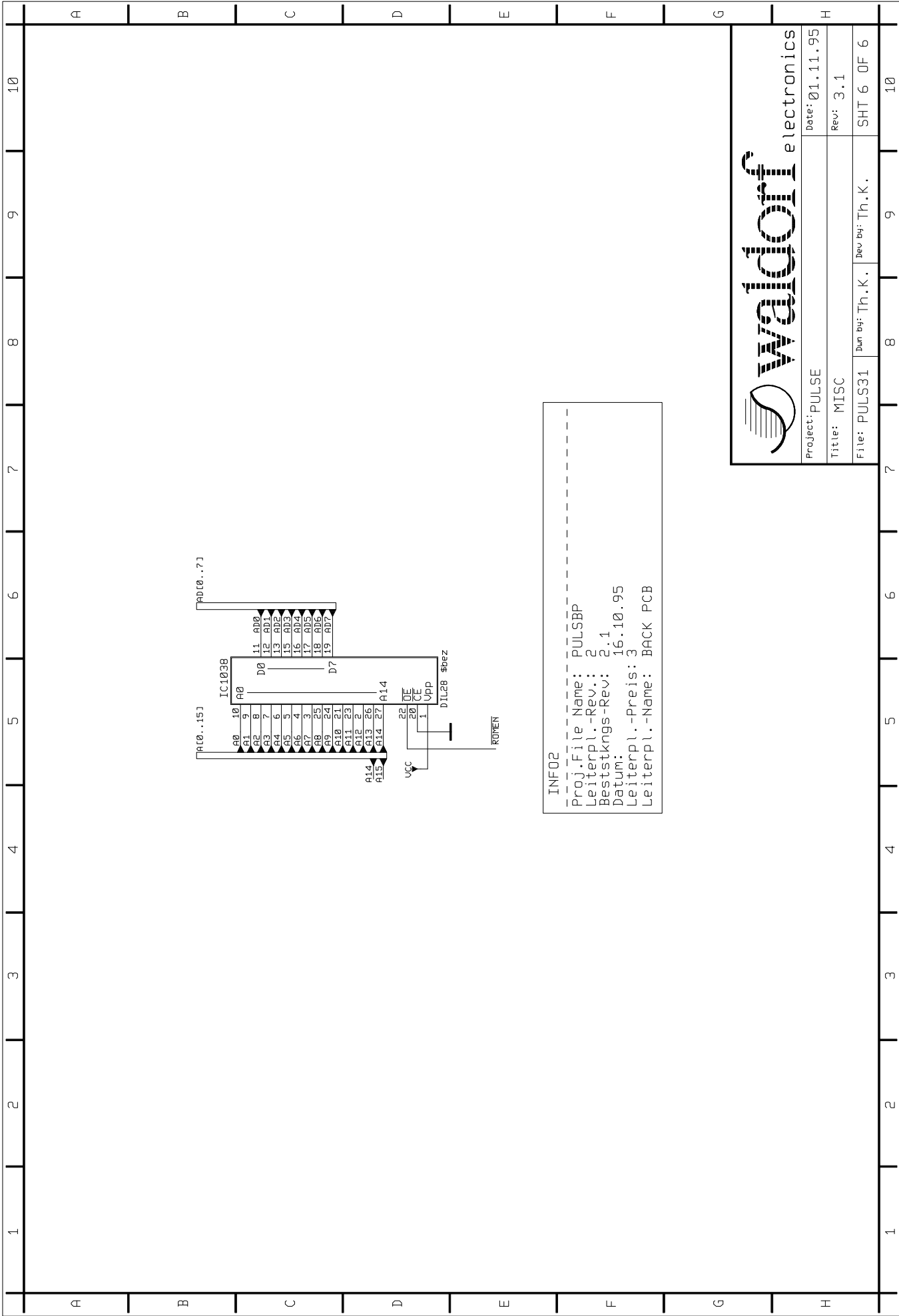




INFO  
 Proj. File Name: PULS31  
 Leiterpl.-Rev.: 3.1  
 Beststckngs-Rev: 3.1  
 Datum: 01.11.95  
 Leiterpl.-Preis: 17  
 Leiterpl.-Name: MAIN PCB

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Project: PULSE  
 Title: POWER SUPPLY  
 Date: 01.11.95  
 Rev: 3.1  
 File: PULS31  
 Dev by: Th.K.  
 SHT 5 OF 6



INFO2  
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 Proj.File Name: PULSBBP  
 Leiterpl.-Rev.: 2  
 Beststkngs-Rev.: 2.1  
 Datum: 16.10.95  
 Leiterpl.-Preis: 3  
 Leiterpl.-Name: BACK PCB

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Project: PULSE Date: 01.11.95  
 Title: MISC Rev: 3.1  
 File: PULS31 Dev by: Th.K. SHT 6 OF 6

## MODIFIKATIONEN

an Leiterplatte PULSE Rev. 3.1:

C4136 10n keramik parallel zu R1008 löten.

Auf der I/O Leiterplatte:

Transil-Diode **BZW06-15B18V** parallel zur DC-Eingangsbuchse löten.





Bestückungsplan PULSBP 16.10.95  
 Leiterpl. Rev. 2 Bestückungsrev. 2.1

