(c) Starting transient in a class C oscillator.
(d) Transient stresses in aircraft structures.
(e) Plastic deformation of eccentric columns.

4. Business management and economic problems:
   (a) Problems related to Air Force program planning.
   (b) Problems related to social security accounting procedures.
5. Problems of a security classified nature for the Atomic Energy Commission and the Armed Forces.

ACKNOWLEDGMENT

Building a large-scale electronic computer such as SEAC from original conception to eventual realization is of course the work of many minds and hands. The successful completion of SEAC at a point in time when its service was of urgent importance to the government was recognized by the Department of Commerce in its Award for Exceptional Service in February, 1951. This citation was awarded to the SEAC staff as a group, and makes particular reference to the individual contributions of W. W. Davis, R. D. Elbourn, A. L. Leiner, S. Lubkin, C. H. Page, J. L. Pike, R. J. Slutz, J. R. Sorrels, and the authors. Special mention should also go to H. Senf and W. Martin for valuable contributions in the early phase of the NBS computer program.

Electronic Circuits of the NAREC Computer*

PAUL C. SHERERTZ†

Summary—**This paper describes several of the circuits developed at the Naval Research Laboratory for its electronic digital computer, the NAREC. These circuits, which include inverters, flip-flops, counters, steppers, pulse generators, adders and comparators, employ crystal diodes where practical for all non-linear functions and use vacuum tubes only where inversion or amplification is required. All circuits are designed to provide low impedance output signals whose maximum and minimum levels are held to prescribed dc potentials. The circuits are packaged in standard 4-tube plug-in chassis in arrangements which make these units functional building blocks of the computer.**

INTRODUCTION

THE NAREC[1] is an electronic digital computer currently being placed in operation by the Naval Research Laboratory. The machine is designed to perform several thousand mathematical operations per second on 11 decimal digit (44 binary digit) numbers, operate in the parallel mode and may be asynchronously controlled to operate at any speed up to its maximum. Cathode-ray tubes and a magnetic drum are employed for high and low speed storage respectively. Information is read into and out of the computer from or to magnetic tape, punched paper tape, or automatic electric typewriters.

A diagram of the computer layout is shown in Fig. 1. Physically, the main frame is divided into the *left* or control section, the *middle* or arithmetic section, the *right* or input-output section and the *bottom* or electrostatic storage section. The magnetic drum is located to the right of the main frame, and a control console is located in front of the *middle* section. Circuit packages are designed to plug in from the front of the frame and are interconnected by horizontal and vertical busses on the back of the frame.

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[1] D. H. Gridley and B. L. Sarahan, "Design of the Naval Research Laboratory Computer," *Elec. Eng.*, vol. 70, p. 111; February, 1951.

As can be seen from the block diagram of Fig. 2, the major portion of the computer is devoted to the task of either storing or transferring numbers. Addition is the only basic mathematical function performed by the computer. Negative numbers are expressed in binary complementary form and subtraction is performed by the addition of negative numbers. Multiplication, division and all other operations are accomplished by a series of shifts and additions or subtractions. Comparators are used to check the transfers between registers and to halt computation when an error is made in the process of a transfer.

The physical realization of the NAREC has resulted in the design of a complete family of digital circuit elements whose inputs, outputs, and constructional features were tailored to the same standards. These devices include gating circuits, vacuum tube registers, pulse generators, stepping elements, counters, parallel adders, inverters, comparators and signal drivers. This report will describe the basic circuits developed for all functions except electrostatic and magnetic storage.

At the time that the electronic design of the NAREC computer was initiated, the following rules were adopted to guide the circuit development:

(a) Where practical, circuits should be designed for dc operation and aperiodic triggering.
(b) Output signal levels should be high enough to permit checking by indicator lights and simple dc measurements.
(c) Crystal diodes should be used in place of vacuum tubes whenever a substantial saving of space or power could be anticipated.
(d) Circuits should be designed to operate at the maximum rate obtainable without the use of complex circuits or heavy duty tubes.
(e) A minimum number of tubes should be used and, where practical, these should be restricted to the

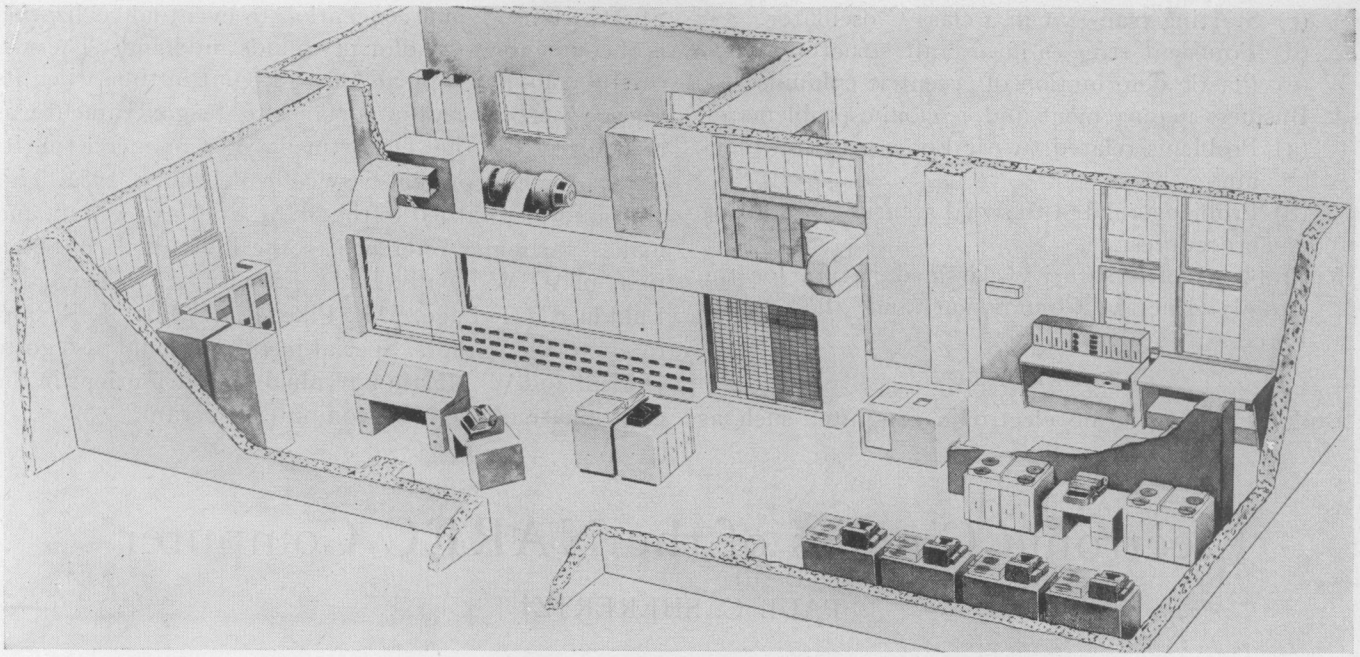

Fig. 1—The NAREC installation.

5670 (or 2C51) and the 5687 dual triodes, and the 6AN5 power pentode.

(f) Circuit design should allow component tolerances of at least five per cent.

(g) Circuits should be designed for plug-in operation.

(h) The outputs of plug-in units should be capable of driving signals with a few-tenths-of-a-microsecond rise time for distances up to 20 feet over open wires without appreciable attenuation.

(i) Plug-in units should contain such circuits as necessary to make the unit a functional building block of the computer.

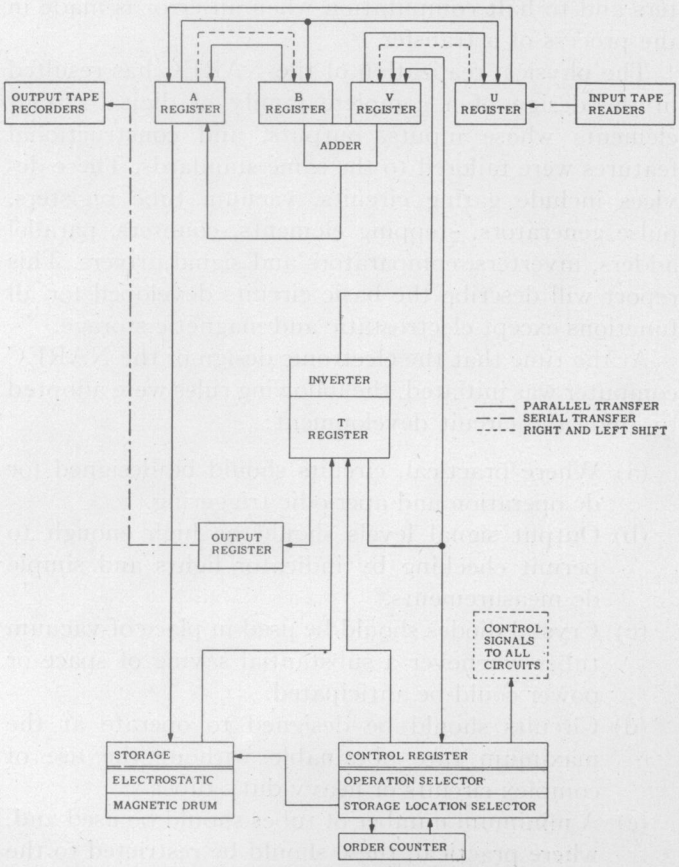

Fig. 2—Block diagram of the NAREC.

The decision to place all electronic circuits on plug-in frames resulted from the view that the servicing of the computer as a whole should consist in locating and replacing faulty units rather than individual faulty components. Thus, the reason for using plug-in units is to speed and simplify servicing rather than to standardize on circuit elements, desirable as this may be. A review of the circuit requirements and available connectors led to the final adoption of the standard chassis shown in Fig. 3, which has a 36-terminal plug, four tubes and space for five neon indicators and 108 components. This type of unit is used for all NAREC circuits except those associated with the electrostatic and magnetic memories. Consideration was given to further subdivision of each plug-in unit into a few standard types of smaller plug-in circuit elements. However, it was decided that this would not appreciably simplify the over-all construction or service problem and might slow down the operation of the circuits by adding capacitance to sensitive signal leads.

Diode Gates

The flow of information within the computer is controlled almost entirely by means of gates. Only two basic types of gates are required to perform all logical selection functions: (1) the "*AND*" gate corresponding to series-connected switches, all of which must be closed to connect the input to the output; and (2) the "*OR*" gate corresponding to parallel-connected switches, only one of which need be closed to connect the input to the output. Logically, the "*AND*" gate indicates that, if all

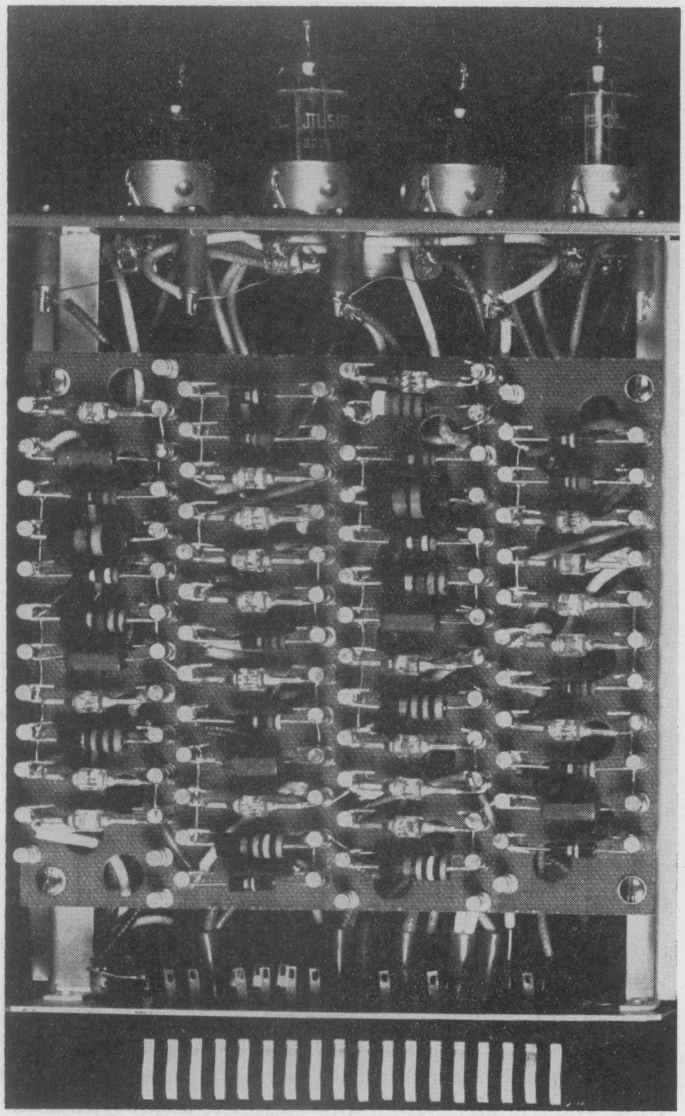

Fig. 3—The standard plug-in chassis.

its inputs (A, B, and . . .) have the value "one," its outputs will have the value "one," while the "*OR*" gate indicates that, if any of its inputs (A or B or . . .) has the value "one," its output will have the value "one." In the NAREC, diodes and resistors are used to make up the gates so that the output of a gate depends on its input potentials. A diode has low resistance when its plate is positive with respect to its cathode, and high resistance when its plate is negative with respect to its cathode. Consequently, in the circuits of Fig. 4(a), the output is held to the more positive of the two input signals A and B, while in the circuits of Fig. 4(b) the output is held to the more negative of the two input signals. The circuits of Fig. 4(a) are indicated symbolically as "*AND*" gates and those of Fig. 4(b) as "*OR*" gates because in the majority of the NAREC circuitry a negative potential represents the value one and a positive potential the value zero.

Crystal rather than vacuum diodes are used in the NAREC for gating and other non-linear functions (such as voltage limiting) that are suited to their characteristics. All crystals used in NAREC circuits were selected to have reverse currents of 0.25 ma or less at 50 volts, negligible drift characteristics and forward resistances of approximately 100 ohms. In the initial design phase of the NAREC it was decided to limit signal amplitudes to a maximum of 50 volts, corresponding to the rated reverse voltage of the crystals, and to a minimum of 30 volts, corresponding to the minimum voltage that would reliably operate a neon indicator. In general, arithmetic circuits such as the registers, adders, comparators and counters were designed for operation with 30-volt signals, while control circuits such as steppers, pulse generators, inverters and drivers were designed with 50-volt signals.

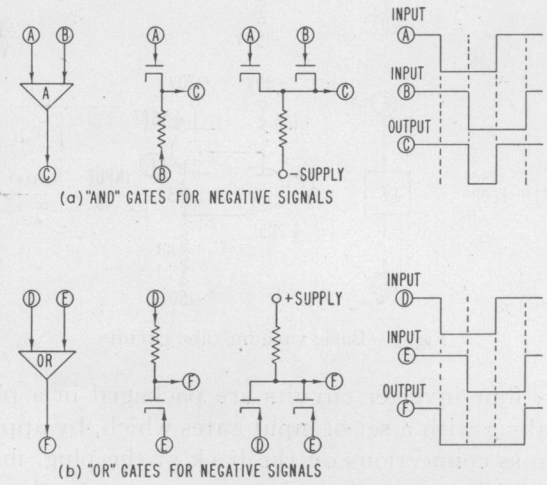

Fig. 4—Diode gates.

Vacuum Tube Circuits

The liberal use of crystal diodes makes it possible to restrict the use of vacuum tubes to functions requiring inversion, voltage amplification, power amplification, or storage. As illustrated in Fig. 5, these functions are ordinarily obtained from triodes connected as inverting amplifiers or cathode followers. The typical NAREC circuit employs dc coupling of high-impedance gate or amplifier outputs to the grid of a cathode follower. Since the cathode follower has a high impedance input and a low impedance output, the amplifier triode may be operated at low currents and voltages in a manner that allows efficient dc coupling without sacrificing high frequency response.

The circuit actually used in the inverter units of the NAREC is shown in Fig. 6. In this circuit the plate load resistor of the amplifier tube is coupled to the positive supply voltage but is limited in its maximum positive excursion to +30 volts by means of diodes. This arrangement permits more rapid response, heavier loading of the cathode follower and higher signal levels for a given current through the amplifier tube, than can be obtained by returning the amplifier plate load resistor directly to +30 volts. The output signal is also limited to a maximum negative excursion of −20 volts by a diode directly on the output bus. For use in the com-

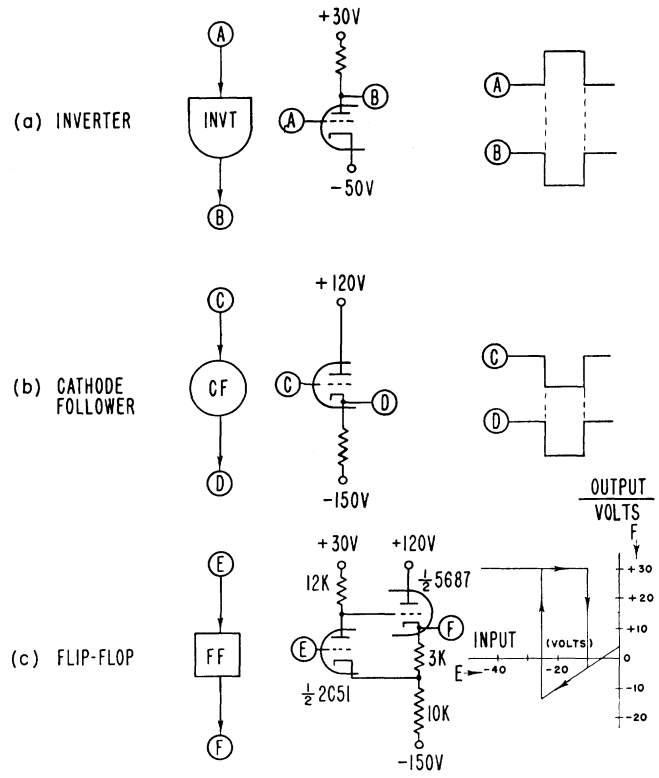

Fig. 5—Basic vacuum tube circuits.

puter, four inverter circuits are packaged in a plug-in unit along with a set of input gates which, by appropriate cross connections on the back of the plug, may be used with any one of the inverters or some other unit.

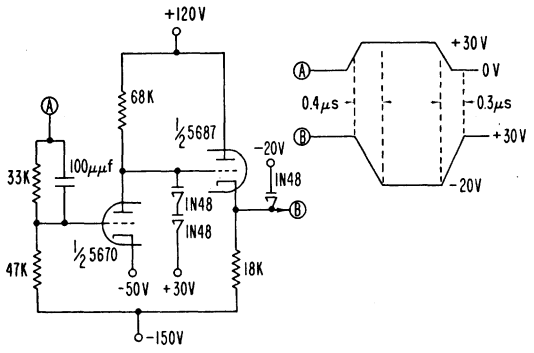

Fig. 6—Inverter circuit.

The most commonly used electronic elements in the NAREC are the single binary digit storage circuits or flip-flops that make up the arithmetic registers. One of these circuits with two input gates, which allow it to be set to the level of either of two input signals, is shown in Fig. 7. The flip-flop itself differs from the basic circuit in that the amplifier plate resistor is returned to the positive supply voltage and that diodes are used to limit the output level to a maximum of +30 volts or a minimum of zero volts. The waveforms included with the schematic diagram illustrate the transfer of information alternately from the two inputs to the flip-flop output. When a transfer is made, a negative reset signal cuts off the amplifier triode and a transfer signal simultaneously connects the plate of the amplifier with a particular in-

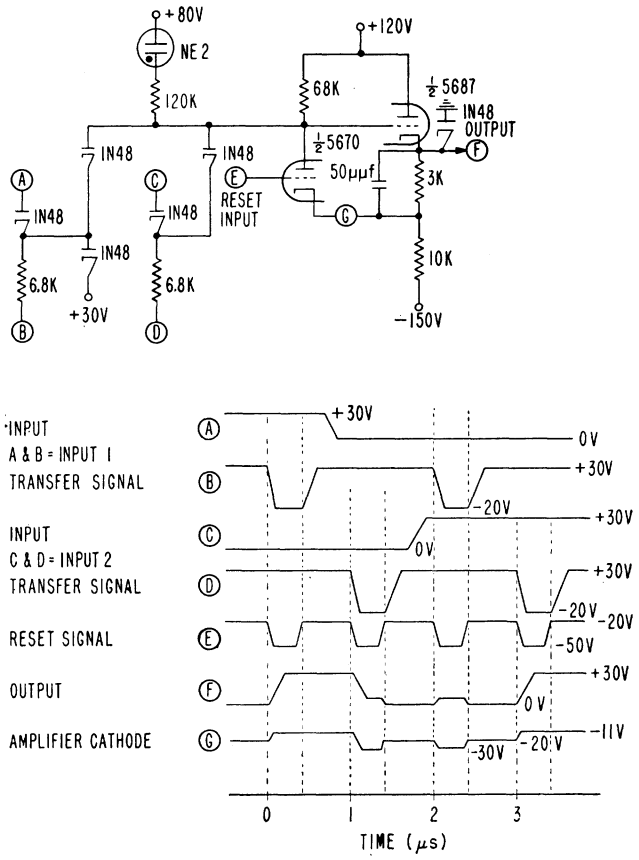

Fig. 7—Schematic diagram of a flip-flop with two input gates.

put through the gates. If the input signal is at +30 volts, the amplifier plate is drawn to +30 volts as soon as the reset signal is applied and remains there when the transfer and reset signals return to their quiescent levels. On the other hand, if the input signal is at zero volts, the transfer signal applied to the input gate holds the amplifier plate to zero volts until after the reset signal has subsided, and the flip-flop output is left at the zero-volt level. For use in the NAREC registers, four flip-flops are packaged in a single plug-in unit together with a total of twenty input gates which permit the transfer of information from five sources into each of the four flip-flops.

The flip-flop can be used as the vacuum tube element of circuits such as counters, steppers, or pulse generators through the addition of appropriate triggering and gating circuitry. Fig. 8 shows a block diagram of a four-stage binary counter and the waveforms of the first two stages. Each counter stage consists of a flip-flop which can be set either positively or negatively by positive rising signals applied to the "set +" or "set −" inputs respectively. The circuitry is so arranged that the "set +" signal overrides the "set −" signal when both are simultaneously present. An *"AND"* gate is used to prevent the "set +" input of the flip-flop from receiving a signal until both the input signal and the flip-flop output are negative. Thus with the flip-flop initially positive, the first positive input pulse will set the output negatively by means of the "set −" signal and the second positive input pulse which reaches both

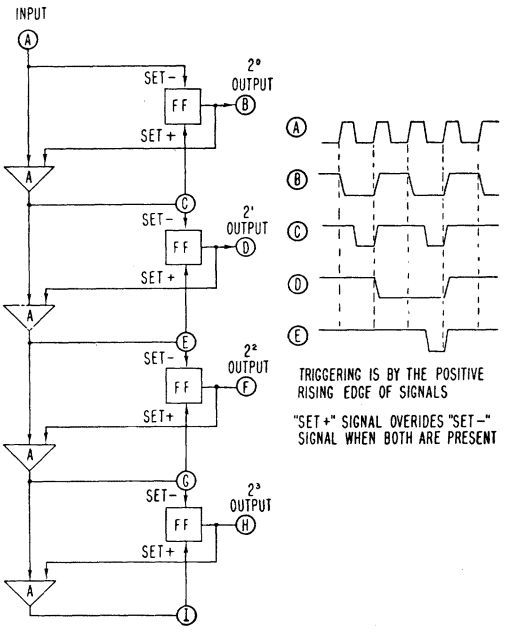

Fig. 8—Binary counter block diagram.

the "set −" and "set +" inputs, will set it positively. To minimize delays in the triggering of successive counter stages, the "set +" signal for one counter stage is also used as the input signal for the following stage. Through this arrangement, each counter in a chain is triggered simultaneously by the rise of the input signal and no cumulative delay occurs.

A binary counter stage operating according to the principles outlined in the block diagram of Fig. 8 is shown schematically in Fig. 9. The flip-flop of the counter is alternately set negatively and positively by positive pulses derived from the positive-rising-edge of the input signal and applied respectively to the grid and cathode of the amplifier triode. The impedances of the "set −" and "set +" trigger circuits are such that the flip-flop will be set positively by the "set +" signal despite the simultaneous presence of a "set −" signal. The maximum counting rate of this type of counter is largely determined by the time constant of the "set +" circuit, and is about one megacycle for the circuit shown. For use in the NAREC, four counter stages are packaged in a single plug-in unit and are connected as indicated in the block diagram so there is no cumulative delay between stages, the delay for any of the four stages being 0.25 microsecond.

A circuit which may be used either as a stepper or as a pulse generator is illustrated in Fig. 10. In principle at least, the circuit is very simple, the flip-flop being set negatively by positive signals applied to the grid of the amplifier triode and set positively, either by the introduction of a negative signal to the amplifier grid, the discharge of a condenser, or a positive signal to the cathode of the cathode follower. When used as a pulse generator, diodes X1, X2, and X5 are biased in a manner that effectively eliminates them from the circuit. In the quiescent state, the amplifier triode is cut off by the biasing arrangement which holds the grid about

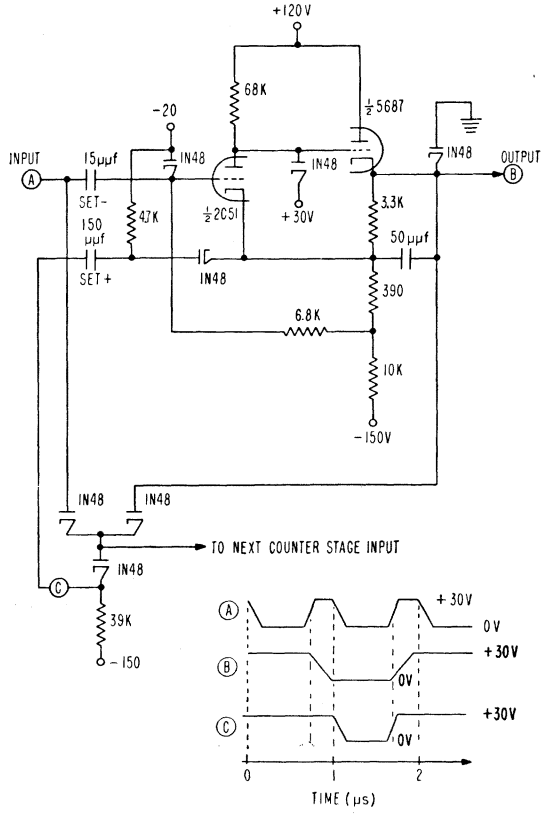

Fig. 9—Binary counter circuit.

four volts negative with respect to the cathode. Introduction of a positive signal to the small input condenser, C1, causes current to flow in the amplifier triode and sets the flip-flop to its negative state. A second con-

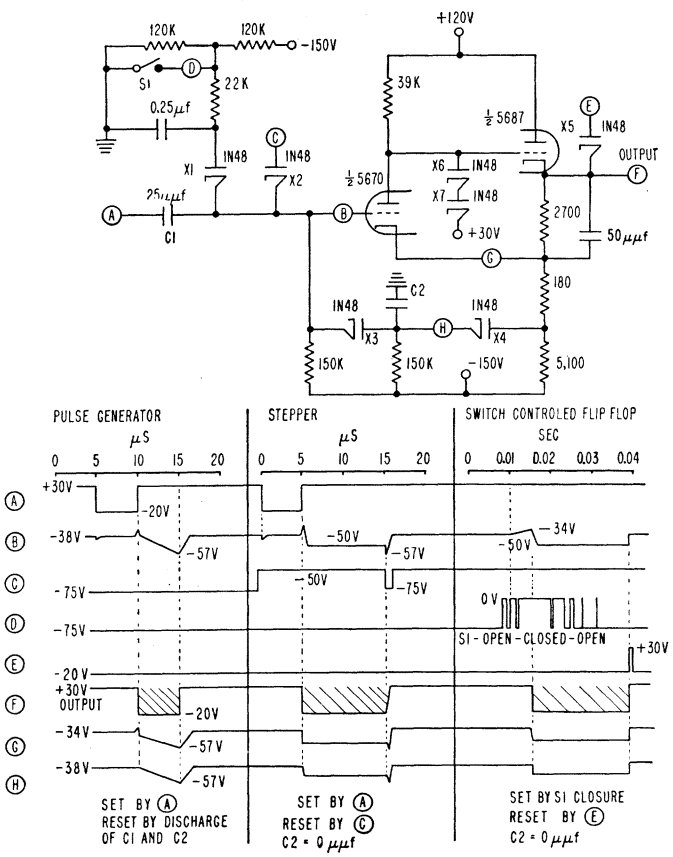

Fig. 10—Pulse generator or stepper circuit.

denser, C2, whose value is chosen to give the desired pulse length, is coupled to the grid of the amplifier triode through a diode, X3. The positive triggering signal is unimpeded by the capacitance of C2 because of the high reverse impedance of X3; however, when the circuit flips to the negative state, the amplifier grid can drop negatively and cut off the triode once more only by discharging both C2 and C1. When the flip-flop has reset to positive state, both condensers C1 and C2 are rapidly recharged by diodes X3 and X4 and low impedance resistance divider in cathode follower output.

In the usual use of the circuit of Fig. 10 as a stepping circuit, C2 is removed, a normally −50 volt "shift" signal is applied to the plate of diode X2, and diodes X1 and X5 are biased to cut off. The flip-flop is triggered negatively by a positive rising signal applied through C1 to the grid of the amplifier triode. Once its output is in the negative state, the flip-flop will not reset because the grid of the amplifier triode is prevented from dropping below −50 volts by the limiting action of diode X2. When it is desired to set the flip-flop positively, the "shift" signal input to this diode is dropped negatively for a time sufficient to permit the discharge of C1 and consequently the resetting of the circuit. If the stepper is part of a ring counter composed of several similar circuits, the output of one circuit (F in Fig. 10) is connected to the input of the next (A in Fig. 10), and the reset or "shift" inputs (C in Fig. 10) of all circuits are connected in parallel. Under this condition a "shift" signal must be long enough to reset a stepper originally in the negative condition, but not long enough to reset a stepper which is triggered to the negative condition during the interval of the "shift" signal. For the circuit illustrated, the "shift" signal should be approximately 0.7 microsecond.

To control the computer it is necessary to transfer information from switches into flip-flops and other circuits. Although this would seem an elementary function, it is complicated by the fact that most switches have appreciable bounce which may last several hundredths of a second. Fig. 10 illustrates one method by which a noisy switch may be made to set a flip-flop. When switch S1 is closed, the input grid of the amplifier triode is raised positively until the circuit is flipped to the negative state. Once triggered, the circuit is held in the negative condition by the signal (−50 volts) applied to the plate of diode X2, despite opening of the switch. Resetting of the flip-flop may be accomplished by raising the level of the potential applied to the plate of diode X5 from −20 volts to +30 volts, or by dropping the potential on diode X2 from −50 to −75 volts.

Aside from the specialized memory and input-output circuitry, the only vacuum tube device in the NAREC which does not employ a dc coupled amplifier, and/or a cathode follower arrangement, is the amplifier driver shown in Fig. 11. The circuit forms the "transfer" and "reset" pulses required to transfer information into flip-flop registers and the "shift" pulses required to step

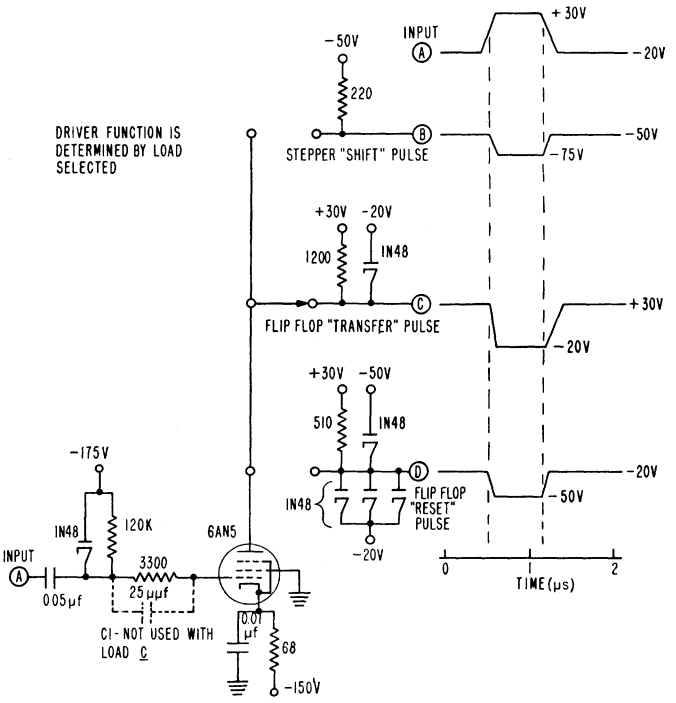

Fig. 11—Amplifier driver circuit.

information in stepper circuits. According to the load used, a single amplifier driver stage is capable of resetting 24 flip-flop register stages, driving 16 register input gates, or shifting the count in a 20-stage ring counter. In effecting the transfer of information between registers, a single pulse is applied to two amplifier drivers, one of which is connected as a "reset" driver, and the other as a "transfer" driver. The "transfer" driver output pulse is caused to lag the output pulse of the "reset" driver by removing the condenser, C1, from the input of this circuit.

Logical Circuits

All of the circuits which have been discussed are constructed on the standard plug-in unit illustrated in Fig. 3. In general, four similar circuits such as flip-flops, inverters, or counters are packaged in a single unit together with such input gating as is required by the NAREC logic and permitted by the available plug connections. A few of the units, however, contain a combination of gates and circuits to modify the input signals according to a particular logic. Three of these circuits, namely the comparator, adder and activator, will be discussed to illustrate the use of gates for controlling circuit operations and to indicate the type of circuit building block formed by a plug-in unit.

A block diagram of a comparator is shown in Fig. 12. Comparison of A against B is made according to the logic that if A *and* B are both negative *or* if A *and* B are both positive, the output of the circuit will be negative. If either A is positive and B negative, or A negative and B positive, the output of the circuit will be positive. Similar comparisons are made for all signal pairs which must be compared and the outputs of all comparators

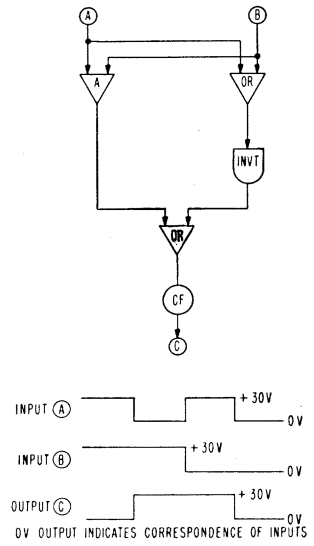

Fig. 12—Comparator block diagram.

are connected in parallel. By this arrangement the output cathode followers act together as a large *"AND"* gate and give a negative output signal only if all signal pairs correspond.

A block diagram of the NAREC adder unit is shown in Fig. 13. This unit contains two logically similar dc coupled parallel adders, the second of which amplifies the output carry signal. The first stage adds the inputs A1, B1, and C1 and develops the digit output D1 and the carry output C2 according to the rules of binary

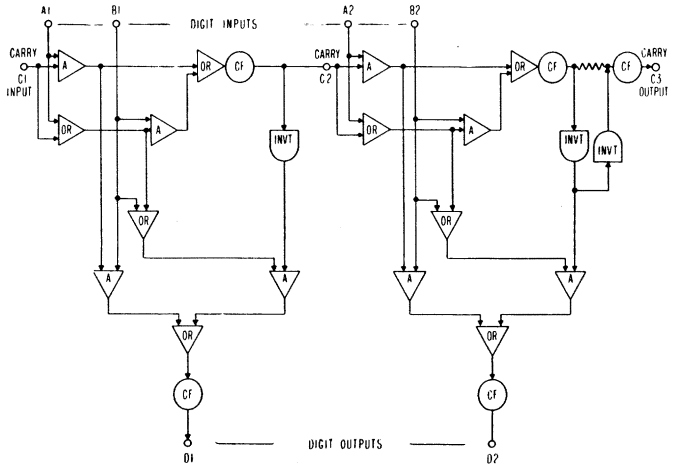

Fig. 13—Block diagram of a two-stage, binary, parallel adder.

addition. A positive potential, nominally +30 volts, represents the binary value "zero" and a negative potential, nominally 0 volts, represents the binary value "one." The gating is arranged so that the carry output C2 will be "one" if [A1 and C1] or [(A1 or C1) and B1] equal "one," and the digit output D1 will be "one" if [A1 or C1 or B1 and not C2] or [(A1 and C1) and B1] are "one." The inversion of carry output C2 is the "not C2" signal. In the second adder stage, the inputs A2 and B2 are added to the carry output (C2) of the first stage to give the digit output D2 and the carry output C3, according to the same logic. Carry output C3 is amplified by means of a double inverter stage to eliminate the attenuation and bias introduced by successive cathode followers and gates. As used in the NAREC, this adder propagates the carry signal with a delay of about 0.05 microsecond per stage.

The various dynamic functions of the NAREC are controlled by compound circuits called activators. One activator is provided for each unique operation (such as the transfer of digits 0 to 12 in the B register to digits 24 to 36 in the A register) directed by the control section of the computer and an order such as multiplication is performed by the successive triggering of several activators. As may be seen in the block diagram of Fig. 14, an activator is basically a stepping circuit with a large number of input selection gates. A cathode follower and gated inverter stage were incorporated in the activator package because these circuits are required to supply signals at the appropriate time and levels to the drivers which actually carry out the functions specified by the activator. Since the stepper circuit of an activator is designed to be triggered by a pulse having a rise time of 0.5 microsecond or less, it is possible to prevent the selection inputs from triggering an activator by slowing their rise time to a minimum of 1.5 microseconds.

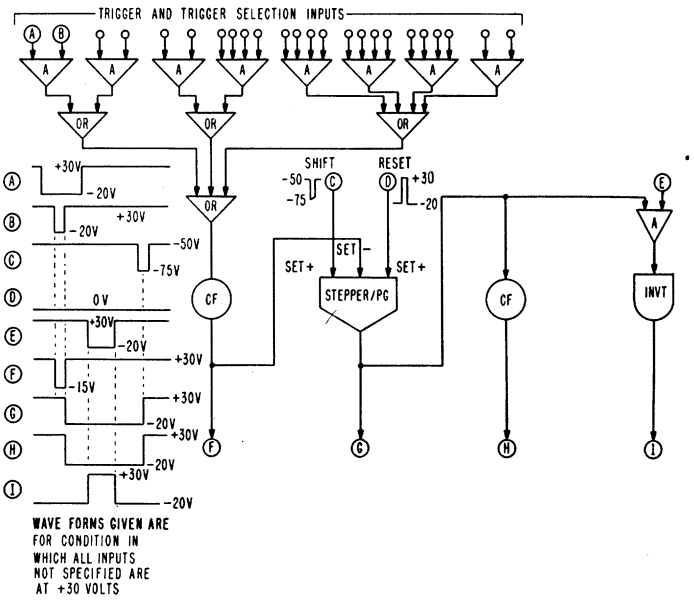

Fig. 14—Activator block diagram.

When an order is to be performed, gated inverters and cathode followers controlled by the order digits of the control register interconnect a set of activators by applying negative selection potentials to one input gate on each. The first activator of the order is triggered to the negative state by a "start" signal. When its function has been performed, it is reset by a "shift" signal which is applied simultaneously to all activators. The resetting of the first activator triggers the second, and the process is continued until the order is completed.

An activator specifying a particular information transfer between two registers also specifies the gating

of the outputs of these registers into inputs of the comparators. The output signal of the comparator then indicates whether the transfer has been correctly made and is used to gate the "shift" pulse applied to the activators. Thus, if the two registers do not contain identical information after the transfer, no "shift" pulse will be transmitted to the activators and the computer will halt on the operation which is in error.

ACKNOWLEDGMENT

The author is indebted to J. J. Fleming and D. H. Gridley for the encouragement and helpful suggestions they have given during the development of these circuits. Much credit should be given A. B. Bligh, E. P. Brown, K. H. Folse and I. J. Levy for their assistance in all phases of the construction, testing and installation of the circuits.

Diagnostic Programs for the Illiac*

DAVID J. WHEELER†, AND JAMES E. ROBERTSON†, ASSOCIATE, IRE

Summary—**The diagnostic programs used for maintenance of the ILLIAC, the University of Illinois' digital computer, are described. The uses of diagnostic programs for fault detection, fault isolation, and periodic computer servicing are discussed. The characteristics of the "leapfrog" program, both as a detection program and as an isolation program, are described in detail. Descriptions of one of the more complex isolation programs and of a typical servicing program are given. Pertinent characteristics of the ILLIAC and techniques of fault isolation are also included.**

INTRODUCTION

THE MAINTENANCE of an electronic digital computer presents unusual problems for the engineer.[1] A computer is a complex collection of elementary circuits. Although the repair of any individual circuit is simple, the location of the particular circuit at fault among the hundreds of faultless circuits poses a problem of major proportions.

Furthermore, the standard of reliability required is an order of magnitude greater than for other electronic apparatus. Fortunately for the engineer, the computer itself can be used as a versatile test instrument for the localization of faults.

In this paper we discuss first the pertinent characteristics and principles of operation of the Illiac. Next, we describe the typical faults which occur and the effects they have on computer operation. Finally, we discuss the use of three types of diagnostic and servicing programs which enable us to use the computer to diagnose its own troubles. These three kinds of programs answer the questions: Is the computer working correctly? Which part of the computer is at fault? How should this analogue control be adjusted?

Because persistent faults can usually be traced easily with a voltmeter, this paper is concerned mainly with intermittent faults. Refined methods are often required for intermittent faults, especially when the error rate is small.

TABLE I

CHARACTERISTICS OF THE ILLIAC

Computer type	parallel, asynchronous, general purpose
Register capacity	40 binary digits
Memory capacity	1,024 words each of 40 binary digits
Number of tubes	
Memory	900
Arithmetic unit	1,100
Control	600
Input-output	100
Total	2,700
Type of instruction	Single address, two instructions per word
Number of digits defining an instruction	8 binary digits
Number of digits defining a memory position	10 binary digits
Operation times	
Multiplication max.	822 μsec
min.	642 μsec
Division	772 μsec
Addition	72 μsec
Input	4 msec per character
Output (punch)	40 msec per character
Total operation time	3,000 hours[1] (approx.)
Tube failures (excluding cathode-ray tubes)	120[1] (approx.)

[1] On April 20, 1953.

CHARACTERISTICS OF THE ILLIAC

The Illiac, which was completed in September, 1952, is the second automatic electronic computer built at the University of Illinois. It is of the same general type as the Institute for Advanced Study computer at Princeton.[2] In particular, it is a parallel computer with an electrostatic Williams memory. The memory is the only synchronous part of the computer, the rest of the control being asynchronous and designed so that the completion of one operation initiates the next. The computer works internally in the binary system and has 40 binary digits

* Decimal classification: 321.375.2. Original manuscript received by the Institute April 27, 1953.

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[1] Other papers discussing the maintenance of digital computers were published in the 1953 Convention Record of the I.R.E.

[2] Descriptions of digital computers similar to the Illiac are given in: G. E. Estrin, "A description of the electronic computer at the Institute for Advanced Study," *Proc. Assoc. for Computing Machinery*, pp. 95–109, Toronto, Ontario, Canada; September, 1952; and R. E. Meagher, and J. P. Nash, "The ordvac," *Rev. Elec. Digital Computers*, pp. 37–43, 1952. (Proc. of Joint AIEE-IRE Computer Conference; December, 1951).