

# TOSHIBA MOS MEMORY PRODUCTS

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**1,024 WORD × 4 BIT CMOS STATIC RAM**  
SILICON GATE CMOS

## TC5514AP-2/-3

## TC5514APL-2/-3

### DESCRIPTION

The TC5514AP is a 4,096 bit high speed and low power random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

The 5514AP is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP is a fully CMOS RAM, therefore it is suited for use in low power applications where

battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL guaranteed a standby current equal to or less than  $1\mu\text{A}$  at  $60^\circ\text{C}$  ambient temperature is available.

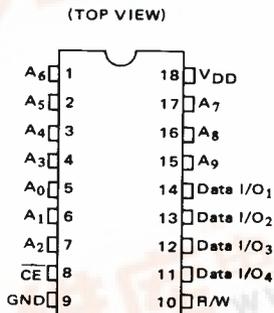
The TC5514AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP is directly TTL compatible in all inputs and outputs.

The TC5514AP is offered in standard 18 pin plastic, 0.3inch in width.

### FEATURES

- Standby Current
  - $0.2\mu\text{A}$  (Max.) at  $T_a=25^\circ\text{C}$
  - $1.0\mu\text{A}$  (Max.) at  $T_a=60^\circ\text{C}$
  - $20\mu\text{A}$  (Max.)
- Low Power Dissipation :  $15\text{mW}$  (Typ.) operating
- Single 5-volt Supply :  $5\text{V} \pm 10\%$
- Data Retention Supply Voltage :  $2 \sim 5.5\text{V}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Access Time
  - $200\text{ns}$  (Max.) : TC5514 AP/APL-2
  - $300\text{ns}$  (Max.) : TC5514 AP/APL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM2114AP Family (Nch 2114 type 4KRAM)
- Package
  - Plastic DIP : TC5514AP/APL

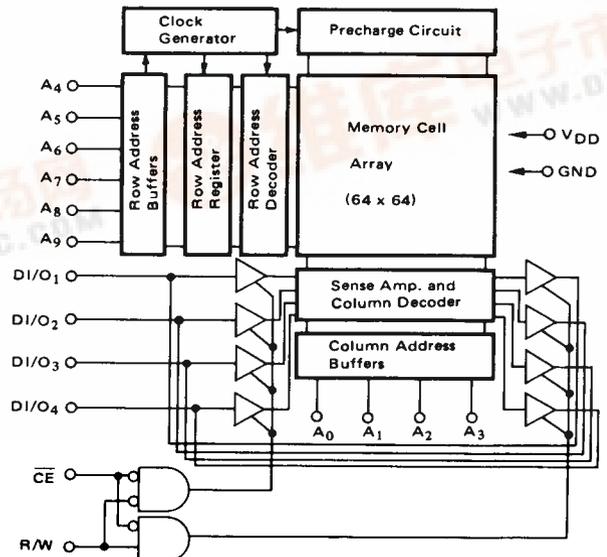
### PIN CONNECTION



### PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Control Input
CE	Chip Enable Input
Data I/O <sub>1-4</sub>	Data Input/Output
V <sub>DD</sub> /GND	Power Supply Terminals

### BLOCK DIAGRAM



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## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3 ~ 7.0	V
V <sub>I/O</sub>	I/O Voltage	0 ~ V <sub>DD</sub>	V
P <sub>D</sub>	Power Dissipation(Ta = 85°C)	550	mW
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C · sec
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	-30 ~ 85	°C

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Level Voltage	2.2	-	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Level Voltage	-0.3	-	0.8	V
V <sub>DH</sub>	Data Retention Voltage	2.0	-	5.5	V

## D.C. CHARACTERISTICS (V<sub>DD</sub> = 5V ± 10%, Ta = -30 ~ 85°C unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. (1)	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-	-	± 1.0	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}, 0V \leq V_{I/O} \leq V_{DD}$	-	-	± 1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	2.0	-	-	mA	
I <sub>DDs</sub>	Standby Current	V <sub>DD</sub> = 2V ~ 5.5V All Inputs = 0.2V or V <sub>DD</sub> - 0.2V	TC5514APL	Ta = 25°C	-	0.2	μA
				Ta = 60°C	-	1.0	μA
					0.05	20	μA
I <sub>DDO1</sub>	Operating Current	t <sub>cycle</sub> = 1μs, I <sub>OUT</sub> = 0mA	-	5.0	9.0	mA	
I <sub>DDO2</sub>		t <sub>cycle</sub> = 1μs, V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = 0V, I <sub>OUT</sub> = 0mA	-	3.0	5.0		

Note (1): V<sub>DD</sub> = 5V, Ta = 25°C

## CAPACITANCE<sup>(2)</sup> (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	-	4	8	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = 0V	-	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

# TC5514AP-2/-3 TC5514APL-2/-3

## A.C. CHARACTERISTICS (V<sub>DD</sub> = 5V ± 10%, T<sub>a</sub> = -30 ~ 85°C)

### • READ CYCLE

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	200	—	300	—	ns
t <sub>ACC</sub>	Access Time	—	200	—	300	ns
t <sub>CO</sub>	$\overline{CE}$ Access Time	—	70	—	100	ns
t <sub>OH</sub>	Output Data Hold Time	15	—	20	—	ns
t <sub>DIS</sub>	Output Disable Time	—	60	—	80	ns
t <sub>COE</sub>	Output Enable Time	5	—	5	—	ns

### • WRITE CYCLE

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	200	—	300	—	ns
t <sub>AW</sub>	Address Setup Time	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	120	—	150	—	ns
t <sub>DS</sub>	Data Setup Time	120	—	150	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	ns

## A.C. TEST CONDITIONS

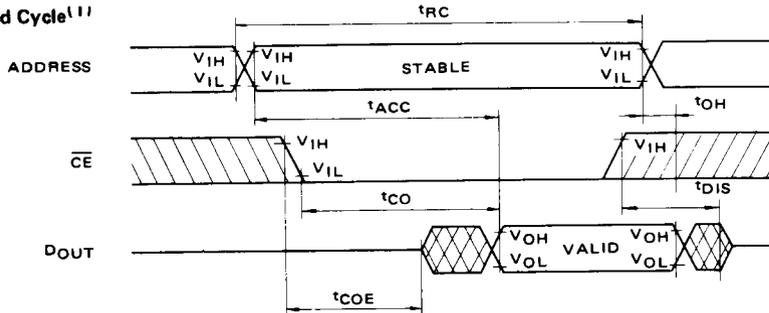
- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

# TC5514AP-2/-3

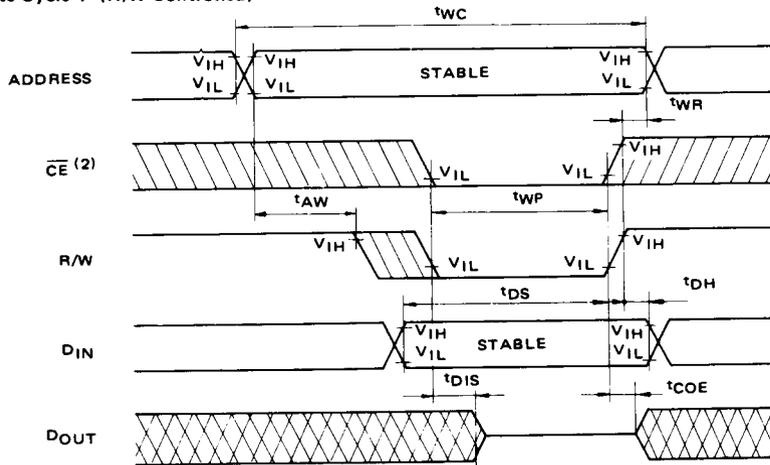
# TC5514APL-2/-3

## TIMING WAVEFORMS

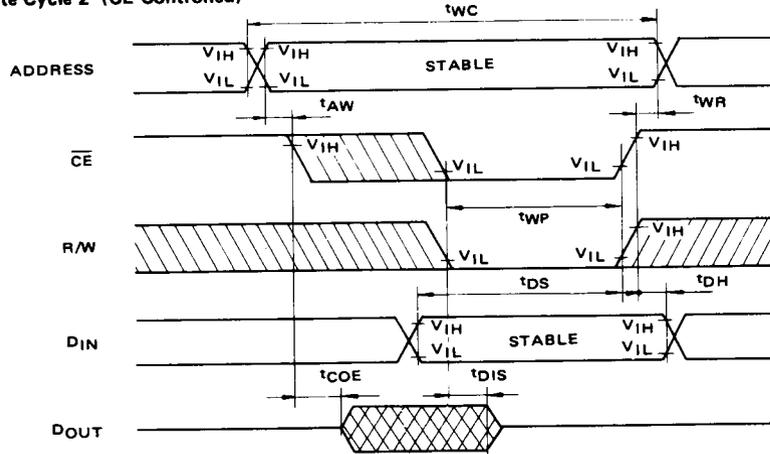
### ● Read Cycle<sup>(1)</sup>



### ● Write Cycle 1 (R/W Controlled)



### ● Write Cycle 2 ( $\overline{CE}$ Controlled)

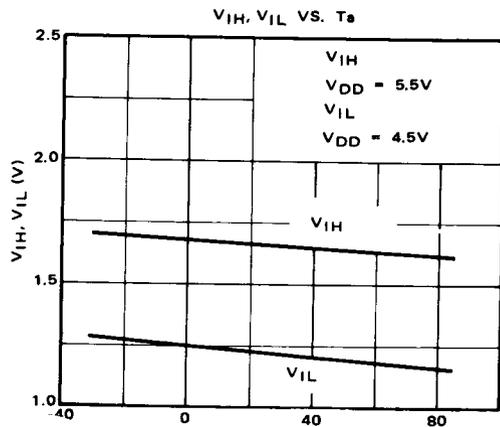
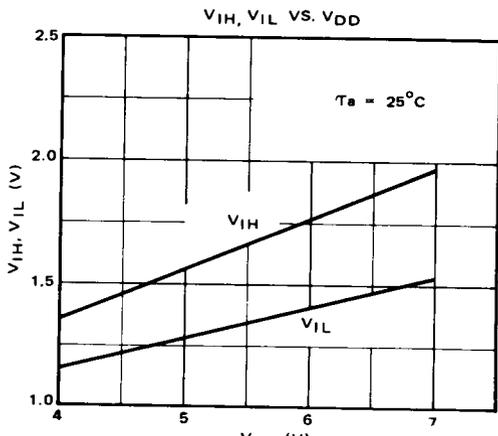
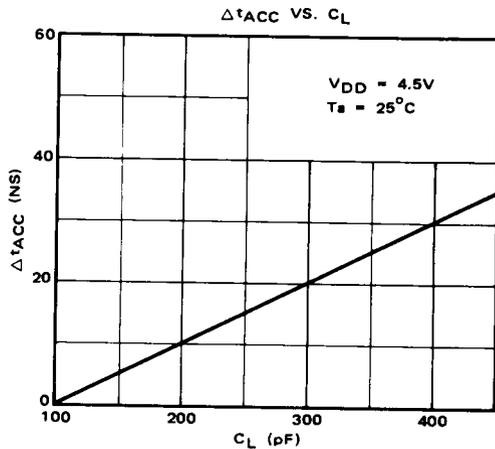
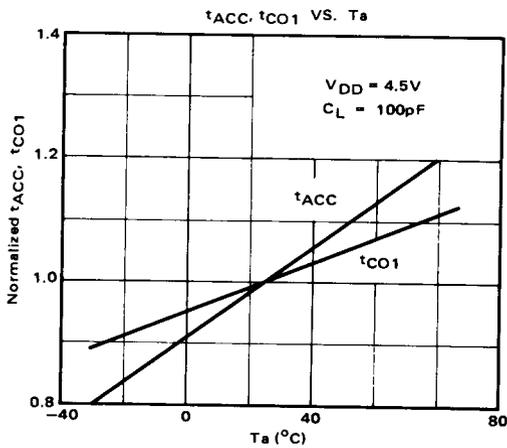
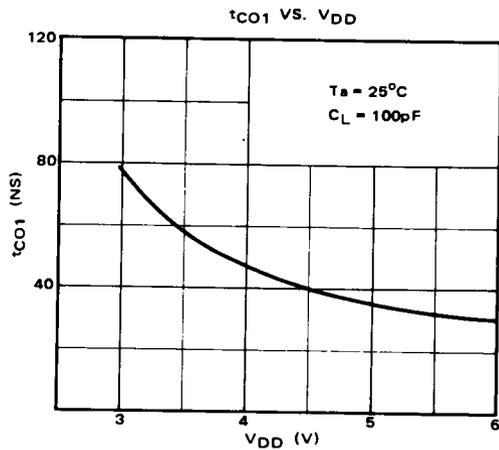
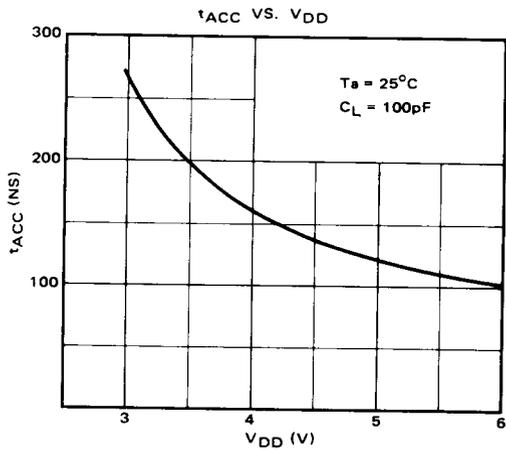


Notes: (1) R/W is high for a Read Cycle.

(2) If the  $\overline{CE}$  low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

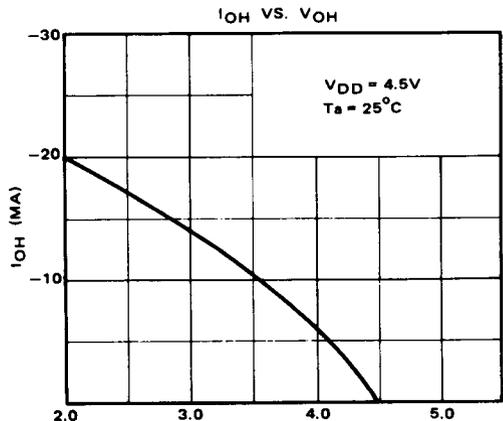
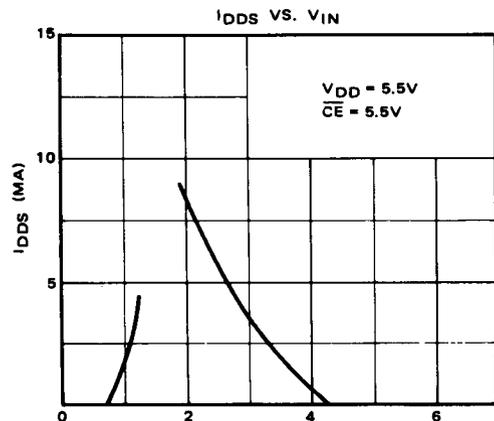
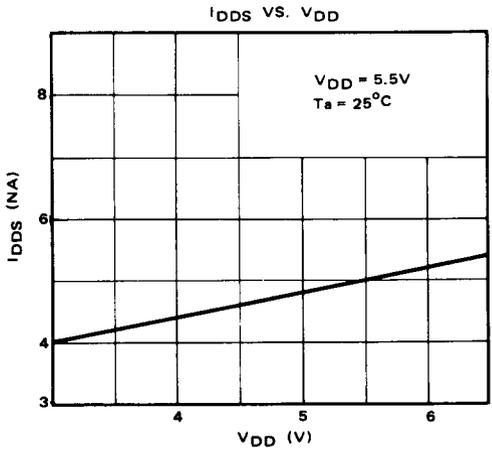
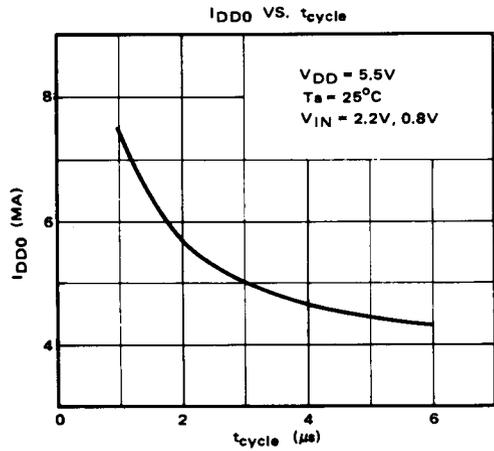
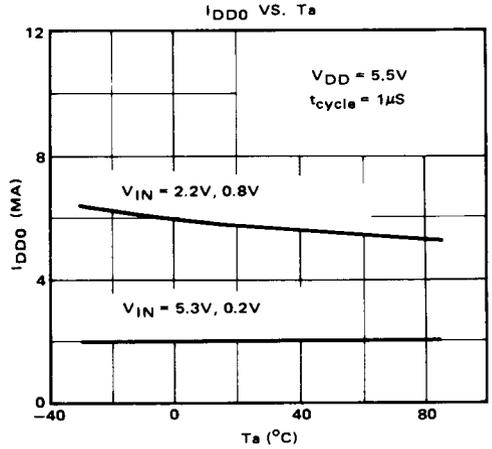
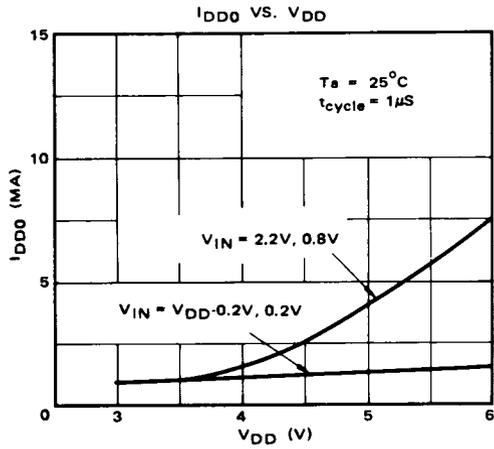
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## TC5514APL-2/-3



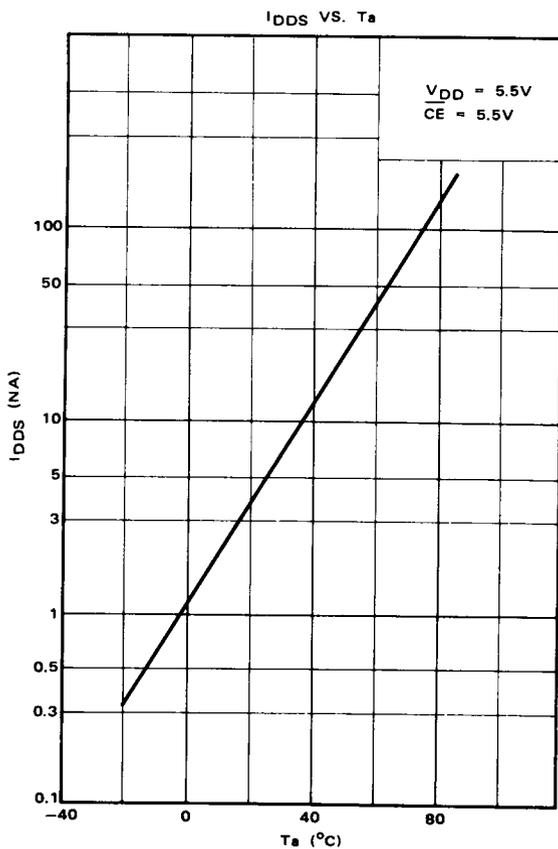
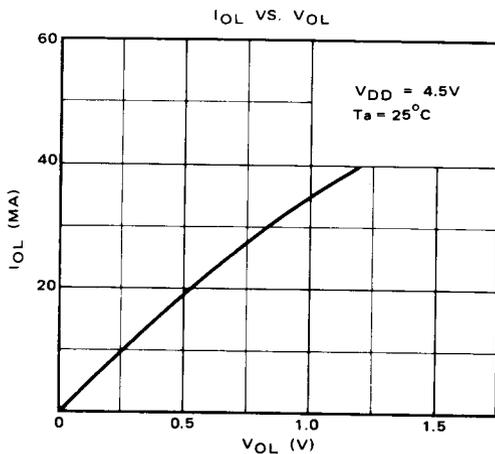
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## TC5514APL-2/-3



# TC5514AP-2/-3

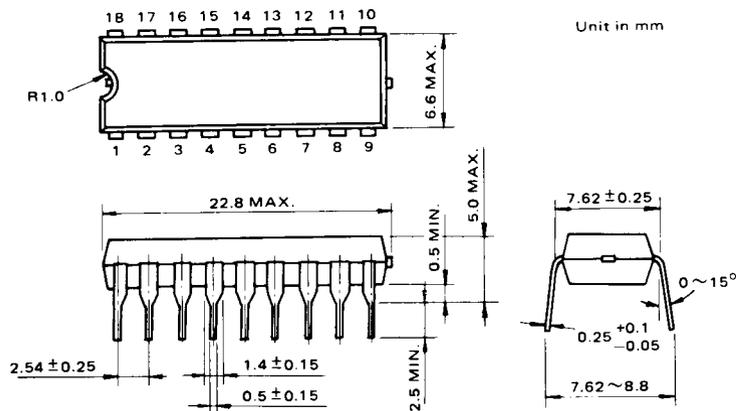
## TC5514APL-2/-3



# TC5514AP-2/-3

# TC5514APL-2/-3

● PLASTIC PACKAGE



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.  
 All dimensions are in millimeters.