PROGRAMMABLE POLYPHONIC SYNTHESIZER

POLY-800II SERVICE MANUAL

CONTENTS

KORG®

1 TECHNICAL SPECIFICATIONS

1. **KEY**
   C – C 49 Keys

2. **MASTER OSC**
   After power ON
   Variation after 0 ~ 10 min.: within ±5 cents
   Variation after 10 min. – 1 hr.: within ±5 cents
   Temperature characteristics 0 – 40°C within ±10 cents

3. **MASTER TUNE**
   #MAX +40 – 70 cents
   bMAX –40 ~ 70 cents

4. **DCO**
   OCTAVE: LOW, MID, HIGH
   WAVE FORM: 16′ + 1/2 8′ + 1/4 4′ + 1/8 2′
   16′ + 8′ + 4′ + 2′
   LEVEL: 0 – 31 32 steps
   DCO 2 INTERVAL: 0 – 12 half-steps 13 steps
   DETUNE: 0 ~ 3
   0, 6.5, 13, 26 cents 4 steps

5. **VCF**
   24 dB/OCT LPF
   CUT OFF: 0 ~ 99 half-steps 100 steps
   RESONANCE: 0 ~ 15 (Q = 0 ~ 10) 16 steps
   KBD TRACK: 0, 50, 100%
   POLARITY:
   EG INT: 0 – 15 16 steps
   CUT OFF = 0 – ±10 OCT (±20%)
   TRIGGER: SINGLE/MULTI

6. **NOISE**
   0 ~ 15 16 steps

7. **EG**
   0 ~ 31 32 steps

8. **MG**
   0 ~ 15 16 steps

9. **DCO MOD**
   BEND : 0 ~ ±730 cents (±30 cents)
   MG : 0 – ±160 cents (±40 cents)
   MG (JOYSTICK): 0 – ±160 cents (±40 cents)

10. **VCF MOD**
    MG: 0 – ±10 2/3 OCT (±10%)
    MG (JOYSTICK): 0 ~ ±10 2/3 OCT (±10%)

11. **EQUALIZER**
    TREBLE: –6 ~ 0 ~ +6 (13 STEP) ±10 dB (±20%)
    ±3 dB POINT:
    2 kHz (±10%)
    BASS: –6 ~ 0 ~ +6 (13 STEP) ±10 dB (±20%)
    ±3 dB POINT:
    300Hz (±10%)

12. **DIGITAL DELAY (DDL)**
    DELAY TIME: 0 – 99 (100 STEP) 4 msec – 1024 msec
    FEED BACK: 0 ~ 15 (16 STEP) 0 ~ 100%
    (until oscillation ceases)
    MOD FREQUENCY: 0 – 31 (32 STEP) 0.1 Hz – 10 Hz
    (±20%)
    MOD INTENSITY: 0 ~ 31 (32 STEP) 1 = 5 TYP
    (1 = 8 MAX)
    EFFECT LEVEL: 0 ~ 15 (16 STEP) 1 = 1 max.
    Effect sound produced

13. **SEQUENCER**
    1 note, rest or tie regarded as 1 step
    maximum of 1,000 steps
    SPEED: 1 step regarded as "♪"
    "♩" = 25 ~ 250 ±20%
    MODE: ONE TIME/REPEAT

14. **TAPE INTERFACE**
    DATA TRANSMISSION SPEED: approx. 2,000 (bit/sec)
    OUTPUT LEVEL: 4.5 mVp-p
    INPUT LEVEL: HIGH 3 Vp-p
    LOW 1 Vp-p

15. **MIDI**
    CHANNEL: 1 – 16 CH
    PROGRAM CHANGE: DISABLE/ENABLE
    SEQUENCER CLOCK: INT/EXT
    SOCKET: IN/OUT

16. **DIMENSIONS**
    780(W) × 286(P) × 87.6(H) mm

17. **WEIGHT**
    4.4 kg (including dry-cell batteries)

18. **ACCESSORIES**
    Pre-load data tape
    Batteries (UM-2 × 6)
    Shielded cord (2.5m × 1)

19. **POWER CONSUMPTION**
    7 W (when using AC adapter)
    SUM-2 × 6 9 V 330 mA ±10%

20. **BATTERY LIFE**
    3.5 hrs. or over (National Hi-Top SUM-2 × 6, continuous usage, 20°C)

21. **EXTERNAL DC POWER RANGE**
    +7.0V ~ +11.0V

22. **ENVIRONMENTAL CONDITIONS**
    Temperature: 0°C ~ 40°C
    Humidity: Below dew point

23. **TIME TO STABLE OPERATION AFTER POWER ON:**
    300 sec.

24. **PERMISSIBLE LINE NOISE VOLUME (with AC adapter)**
    5 min. marked without malfunction at positive polarity
    90°, 350 ns, 500 V pulse

25. **ELECTROSTATIC TEST**
    Normal function at 10 kV of static electricity

26. **ENCLOSURE HEAT BUILD-UP**
    15 or less

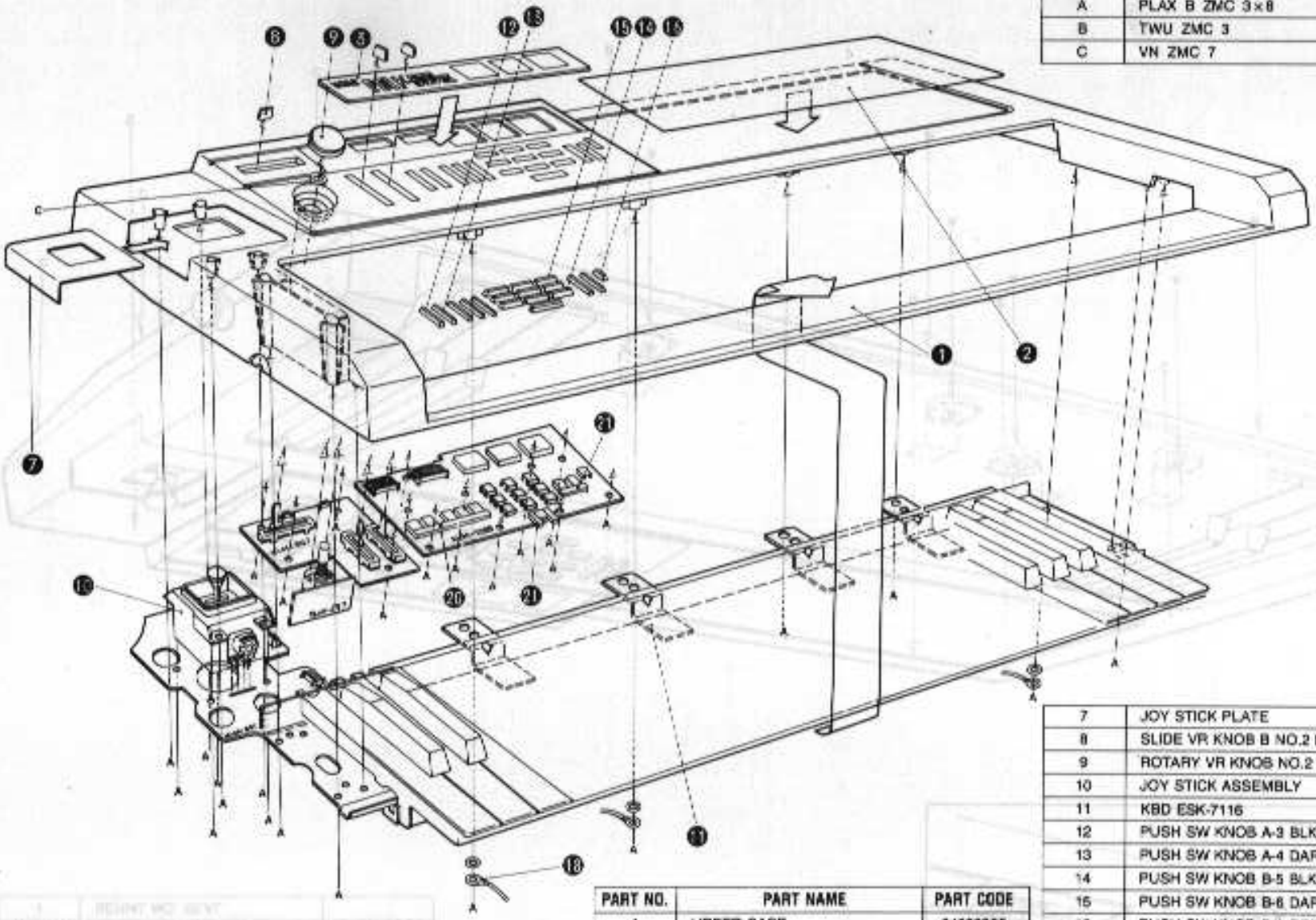
27. **AT POWER ON/OFF**
    spike noise — less than 300 mVp-p

28. **OUTPUT LEVEL (Line Out)**
    C4 – C5 8 notes output simultaneously, VOL MAX,
    –6dBm (±3dB)

29. **NOISE LEVEL**
    JIS-A AVERAGE

	GATE ON	GATE OFF
DDL ON	–76 dBm TYP (–70 dBm MAX)	–90 dBm TYP (–84 dBm MAX)
DDL OFF	–80 dBm TYP (–74 dBm MAX)	–90 dBm TYP (–84 dBm MAX)

30. **ELECTRICAL WAVE INTERFERENCE**
    FCC (U.S.A.)
    VDE (W. Germany)
    Certification for each under review.

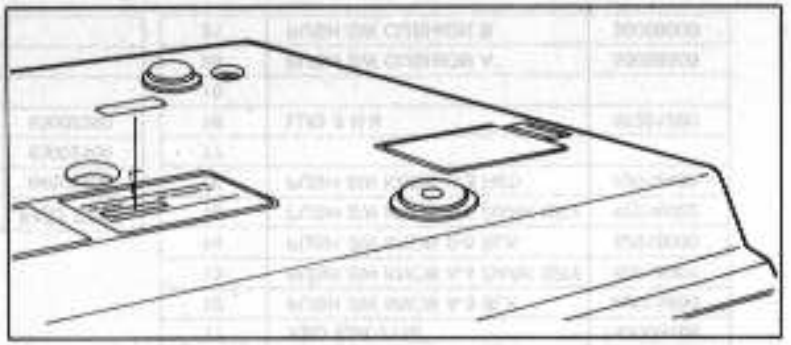


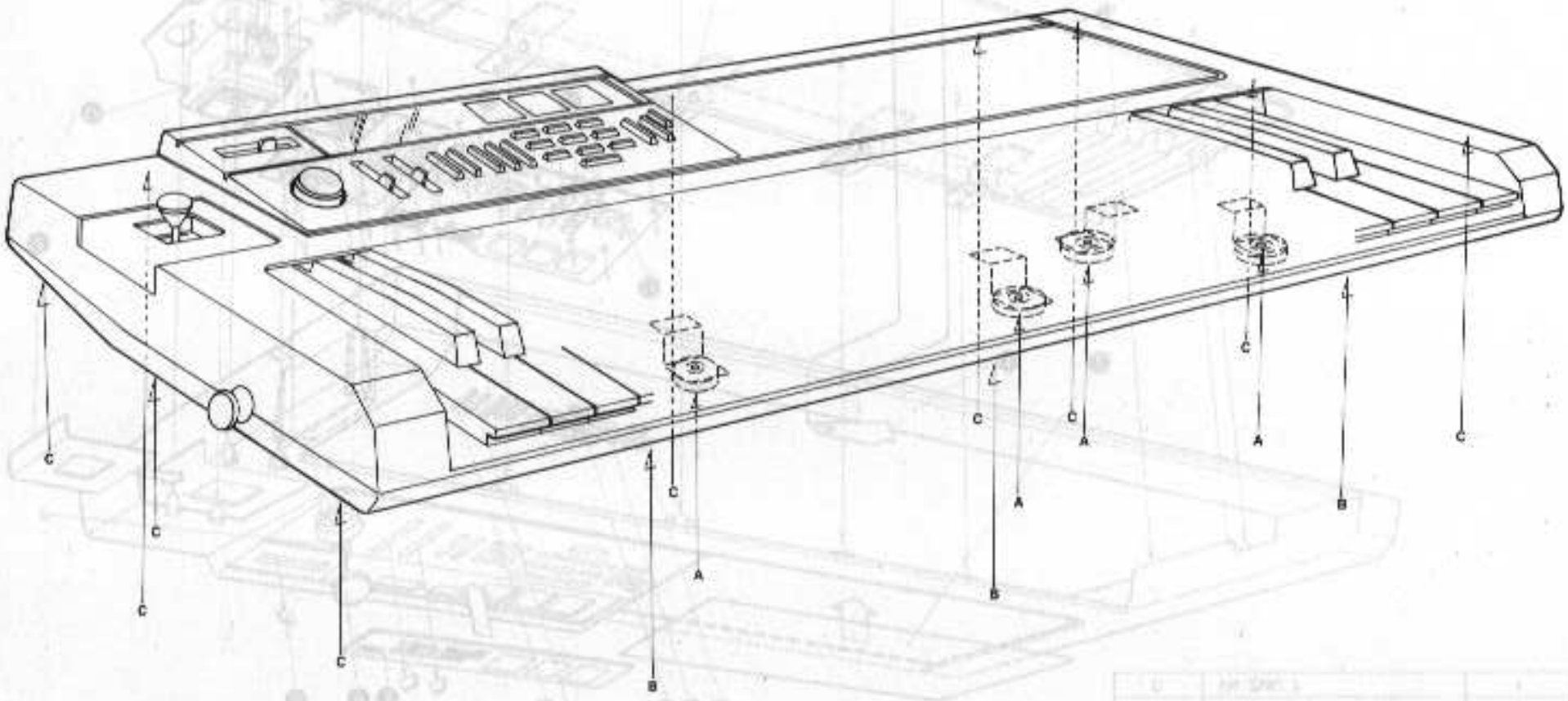
PART NO.	SCREWS, NUT	Q'TY
A	PLAX B ZMC 3×8	29
B	TWU ZMC 3	3
C	VN ZMC 7	1

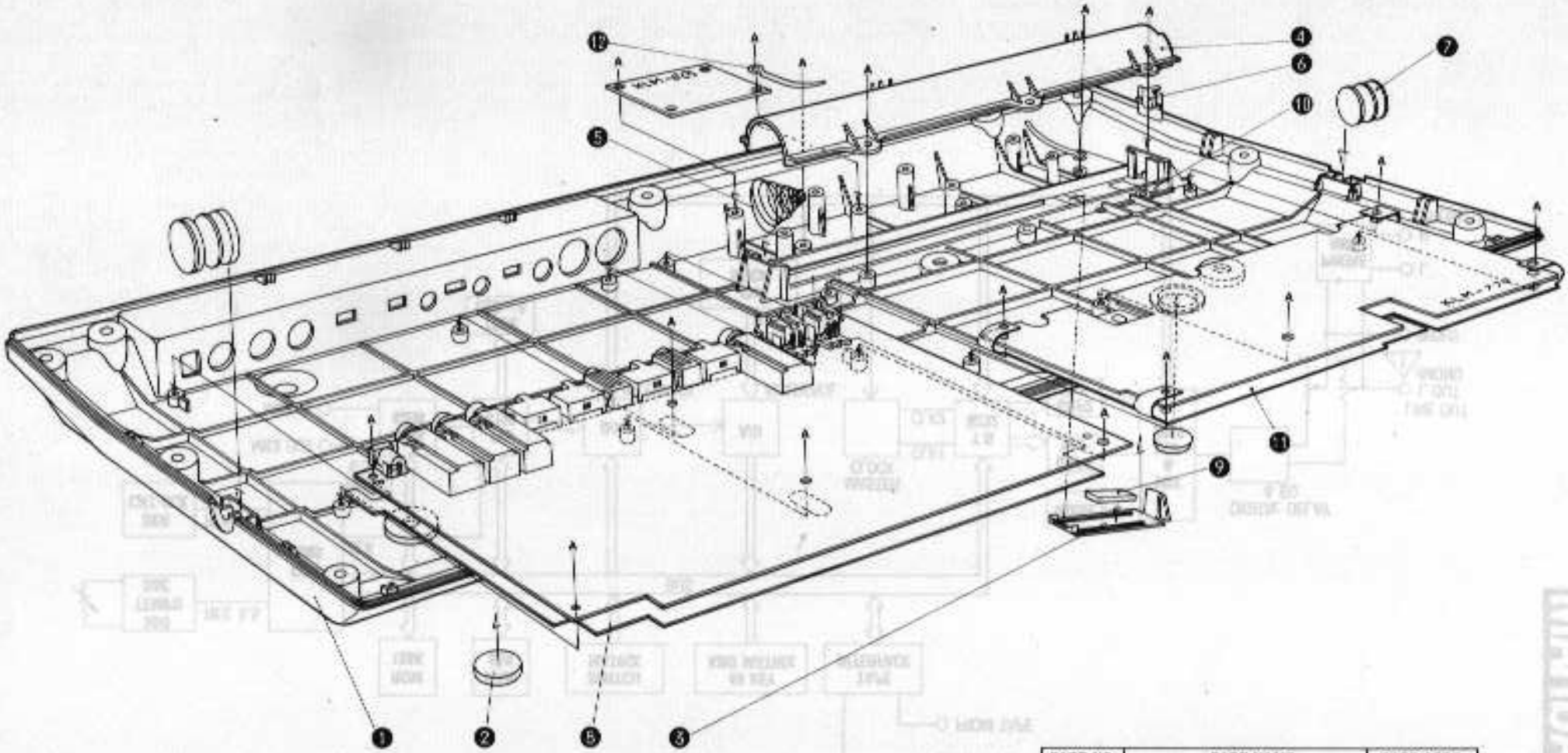
PART NO.	PART NAME	PART CODE
1	UPPER CASE	64620900
2	PARAMETER INDEX SHEET	63002400
3	LED DISPLAY COVER	63002300
4		
5		
6		
7	JOY STICK PLATE	64062600
8	SLIDE VR KNOB B NO.2 BLK	62015600
9	ROTARY VR KNOB NO.2 BLK	62015700
10	JOY STICK ASSEMBLY	
11	KBD ESK-7116	42003100
12	PUSH SW KNOB A-3 BLK	62015900
13	PUSH SW KNOB A-4 DARK GRY	62015901
14	PUSH SW KNOB B-5 BLK	62016000
15	PUSH SW KNOB B-6 DARK GRY	62016002
16	PUSH SW KNOB B-3 RED	62012402
17		
18	LUG 3 N-3	67201200
19		
20	PUSH SW CUSHION A	50006900
21	PUSH SW CUSHION B	50009000

PART NO.	SCREWS	Q'TY
A	FE B BZMC 5×8	4
B	PLAX B BZMC 4×8	3
C	PLAX B BZMC 4×12	9

PART NO.	PART NAME	PART CODE
1	SERIAL NO. SEAL	



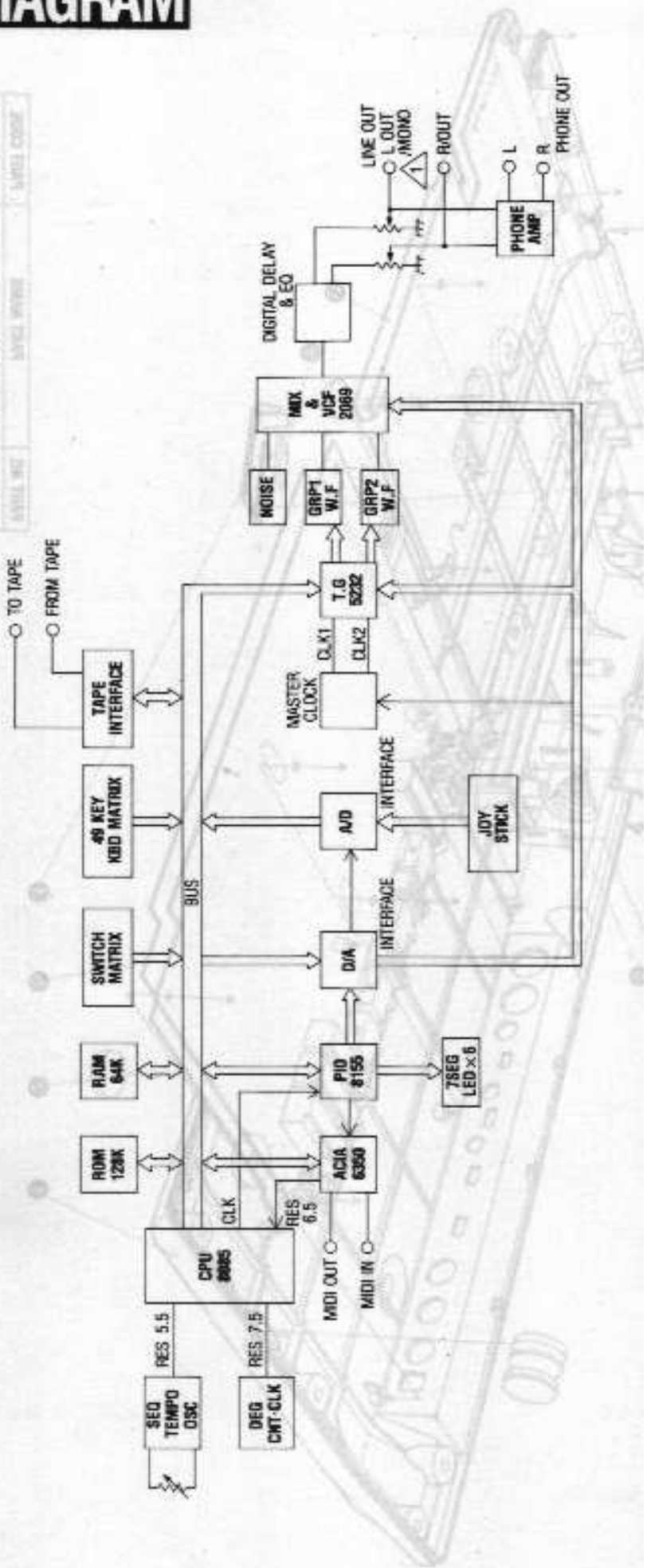


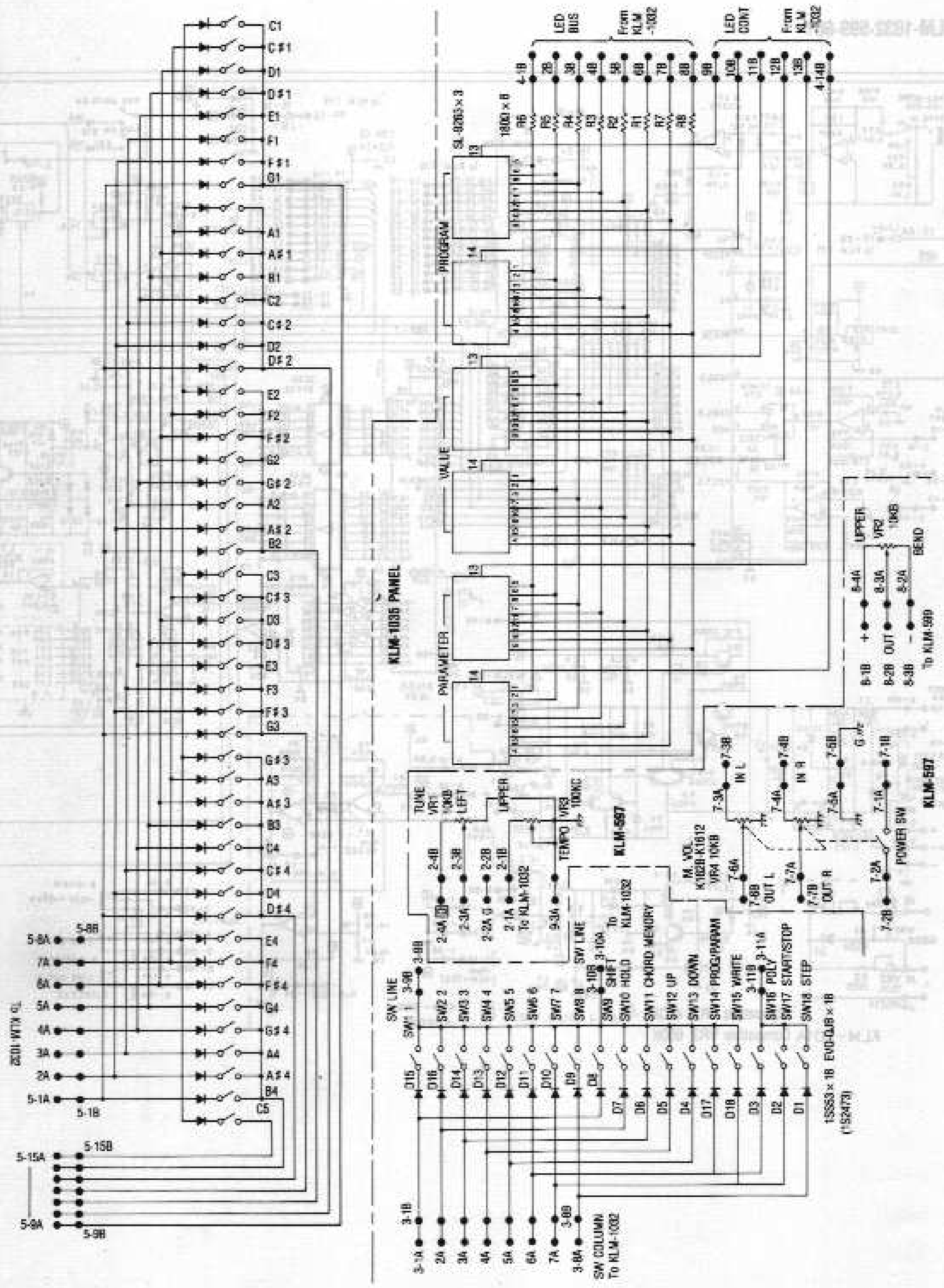


PART NO.	PART NAME	PART CODE
1	LOWER CASE	64621000
2	RUBBER FEET	50008700
3	BATTERY COVER	64621100
4	BATTERY HOLDER	64621200
5	BATTERY TERMINAL (−)	64058100
6	BATTERY TERMINAL (+)	64058101
7	STRAP PEG	64402200
8	SHIELDING SHEET	58018004
9	BATTERY CUSHION 16×30×4	50006800
10	RIBBON	54006100
11	SHIELDING SHEET	63002500
12	SPIRAL CLIP CS-8	54006600

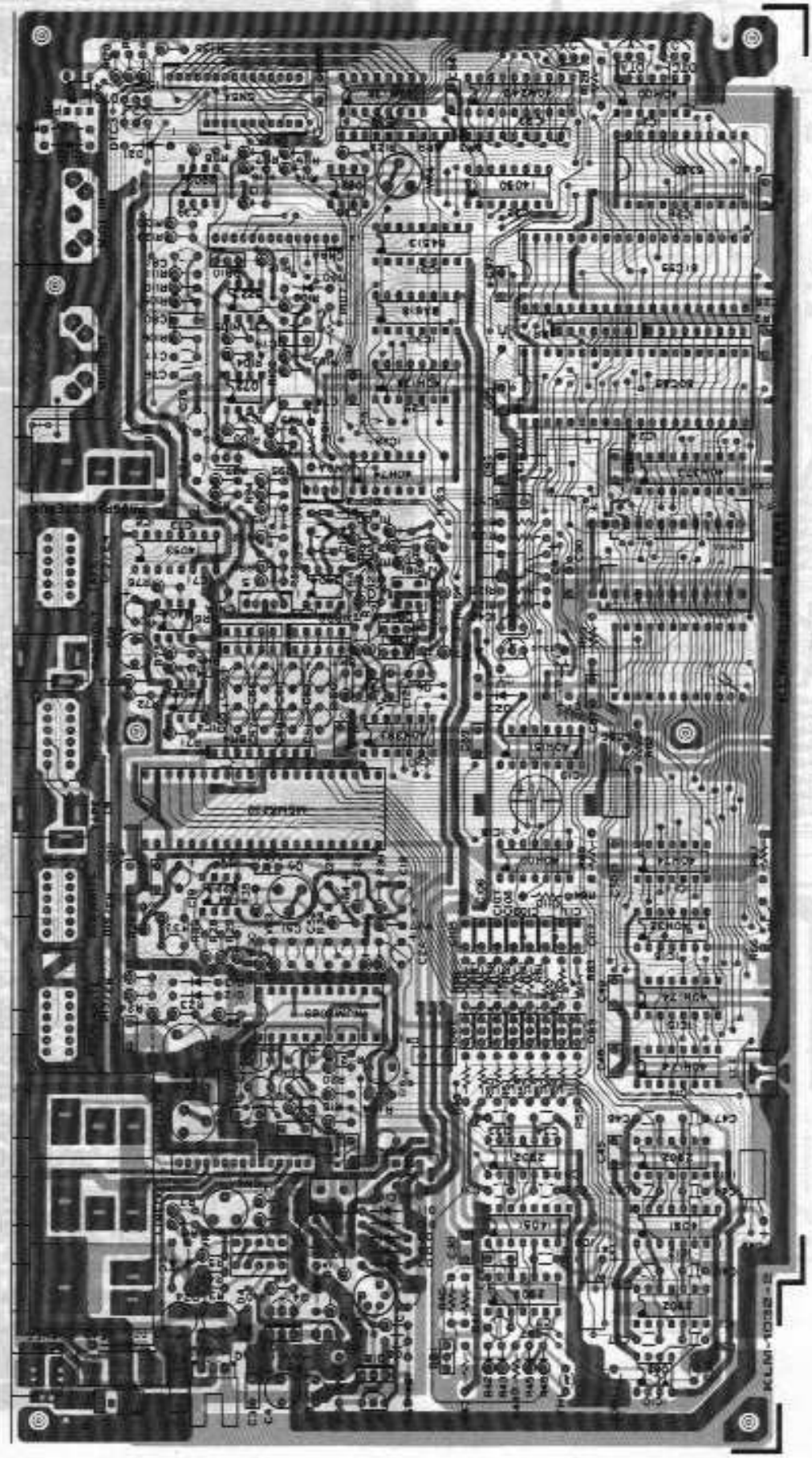
PART NO.	SCREWS	Q'TY
A	PLAX B ZMC 3×8	18

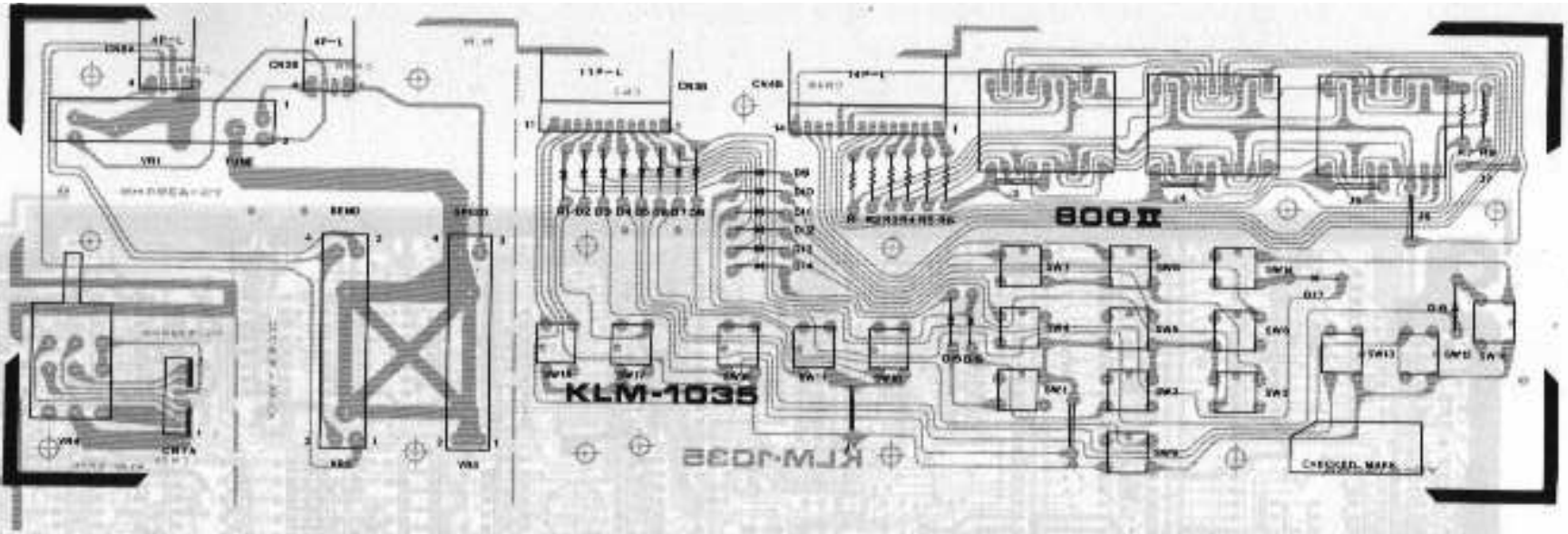
4. BLOCK DIAGRAM

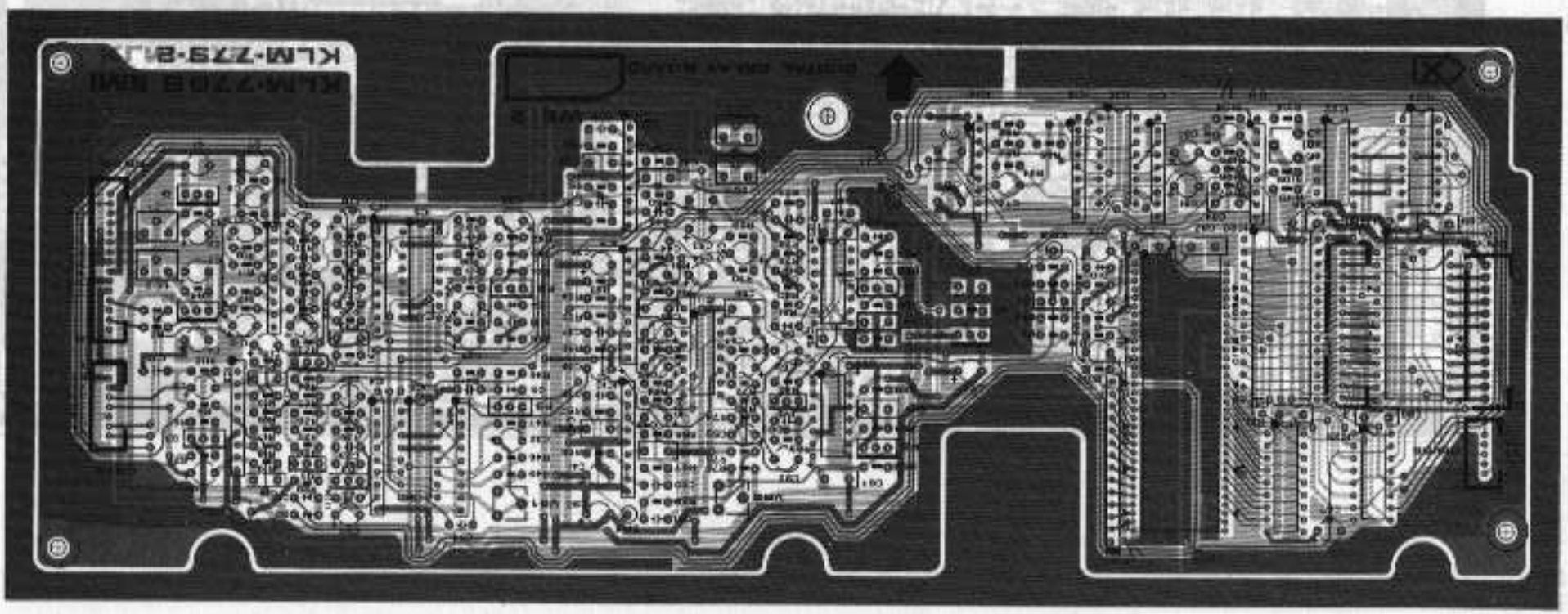


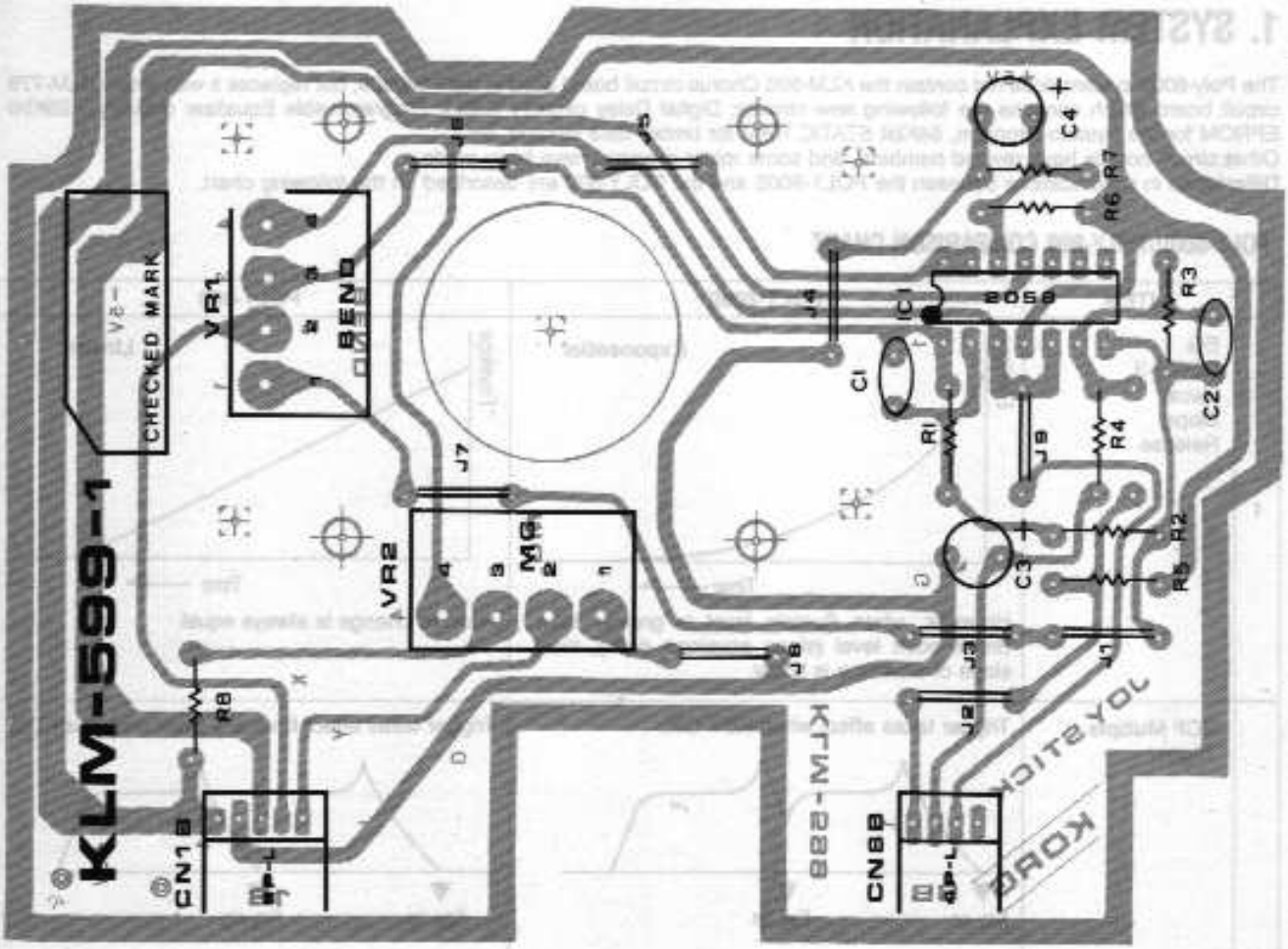

C1
C♯1
D1
D♯1
E1
F1
F♯1
G1
A1
A♯1
B1
C2
C♯2
D2
D♯2
E2
F2
F♯2
G2
G♯2
A2
A♯2
B2
C3
C♯3
D3
D♯3
E3
F3
F♯3
G3
G♯3
A3
A♯3
B3
C4
C♯4
D4
D♯4
E4
F4
F♯4
G4
G♯4
A4
A♯4
B4
C5
5-8A
7A
6A
5A
4A
3A
2A
5-1A
5-8B
5-1B
5-15A
5-15B
5-9A
5-9B

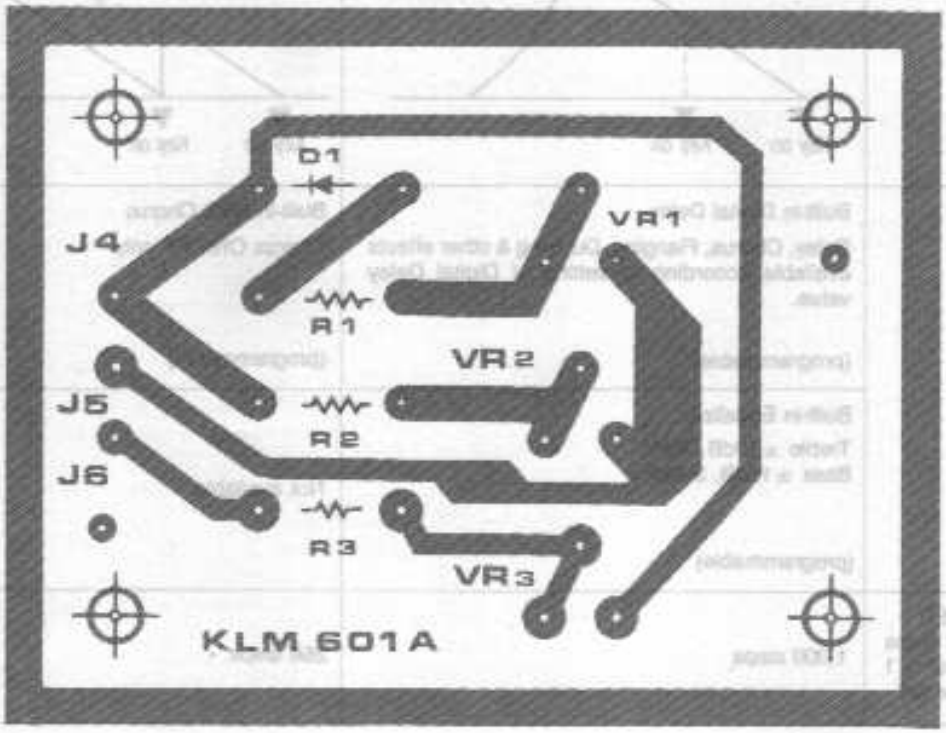
6. P.C. BOARD




KLM-1035
800II




KLM-599-1
CHECKED MARK
VR1
BEND
VR2
MG
J7
J8
J4
J9
J3
J2
J1
C1
C2
C3
C4
R1
R2
R3
R4
R5
R6
R7
R8
CN1
CN2
4P-L
2050
KLM-588

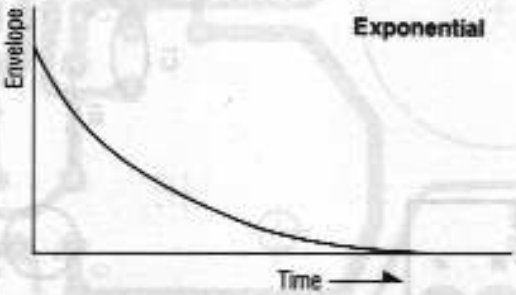
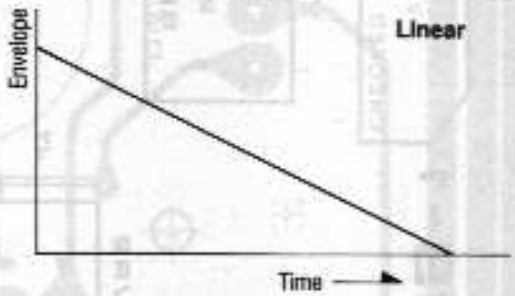
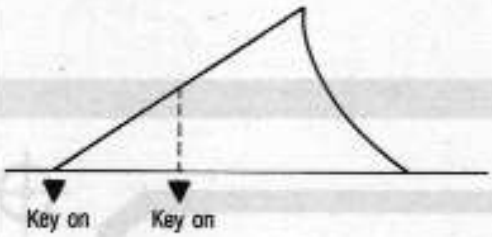
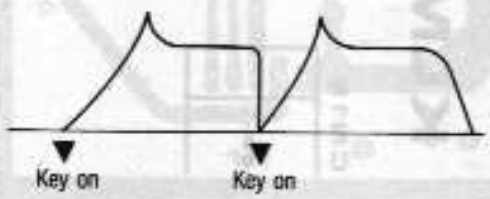
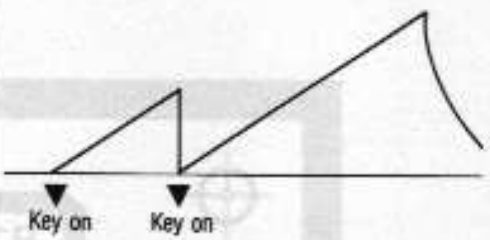

D1
VR1
J4
R1
VR2
J5
R2
J6
R3
VR3
KLM-601A

7. CIRCUIT DESCRIPTIONS

1. SYSTEM EXPLANATION

The Poly-800II system does not contain the KLM-598 Chorus circuit board used in the Poly-800, but replaces it with a new KLM-779 circuit board which contains the following new circuits; Digital Delay circuitry (DDL), Programmable Equalizer circuitry, 128Kbit EPROM for the System Program, 64Kbit STATIC RAM for timbre data storage, etc.
Other circuit boards have revised numbers, and some minor changes have been made.
Differences in specifications between the POLY-800II and the POLY-800 are described on the following chart.

POLY-800II/POLY-800 COMPARISON CHART

	ITEM	POLY-800II	POLY-800
1	EG DEG 1-3 Decay Slope Release	Exponential  However, when Sustain level is greater than Break point level (slope envelope rises), then slope of envelope is linear.	Linear  Ratio of change is always equal
2	VCF Multiple Trigger	Trigger takes effect when KEY ON.  	Trigger takes effect from any point when Key ON.  
3	EFFECT	Built-in Digital Delay Delay, Chorus, Flanging, Dubbing & other effects available according to setting of Digital Delay value. (programmable)	Built-in BBD Chorus Chorus ON/OFF only (programmable)
		Built-in Equalizer Treble ±10dB, 2kHz Bass ±10dB, 300kHz (programmable)	Not available
4	SEQUENCER Max. no. of steps (1 step equal to 1 note, rest or tie)	1,000 steps	256 steps

	ITEM	POLY-800II	POLY-800
5	DATA BACKUP		
	SEQ MODE	One-time repeat Back up	Not available
	SEQ CLOCK INT/EXT	Back up	INT fixed at power ON
	MIDI CHANNEL	Back up	Back up
	PROG CHANGE	Back up	Disable at power ON
6	MIDI SPECIFICATIONS		
	CHANNEL	Channel selection available in SEND or RECEIVE, however SEQ data fixed at CH 2. OMNI ON until parameter 87 is called.	Channel selection available only at RECEIVE. Note data fixed at CH 1, SEQ data at CH 2. OMNI ON until parameter 86 is called.
	MODE MESSAGES	Reception only OMNI ON/OFF	Sends OMNI OFF, POLY ON at SEQ START Sends OMNI ON, POLY ON at SEQ STOP
	DATA DUMP	SEND/RECEIVE OF DATA DUMP	Not available with POLY-800 alone.

2. MAIN CIRCUIT EXPLANATION

KEYBOARD DATA PROCESSING AND PANEL SWITCH OPERATION

There are six 8-tone keyboard buses (plus 1 tone for high C). IC34 decodes addresses for CPU bus line supply.
Key on/off data is read by the CPU via the IC33 buffer.
When the CPU receives key data, it instantly outputs pitch data to the TG. (Tone Generator)
Note; If IC34 (TC40H138) fails, then there will be no sound for some of all groups of eight notes. If IC33 (TC40H240) fails then sound will not be heard for every eighth note.
Switch operation is exactly the same as the keyboard.
DC01 and DC02 octave switching is read by the CPU via matrix circuit and performed by IC3 (MSM5232) itself. The MSM5232 output goes through waveform synthesis circuit (which includes IC's 4, 5, and 6) and is input to filter chip IC1 (NJM2069).
Likewise, EG (DEG1, DEG2, DEG3), LEVEL1, LEVEL2, CUTOFF, and other switching is read by the CPU via the same matrix. The CPU processes the data and controls IC2069 via a D/A converter and time sharing CV circuit.

Data of sounds created by the user is stored in static RAM KLM-779 IC20 (MPD4464). Therefore, to maintain all program data when the unit is turned off, it is necessary for this type of memory to have a battery have a battery backup. Although the system does contain a built-in lithium battery to protect the memory, it is housed in the main circuit board KLM-1032 — not in KLM-779 which contains the RAM. Consequently, if the KLM-779 is disconnected, timbre data will be erased.
As for the delay circuitry, a Gate Array (MPD65010 CW-113), such as is used in the DW-8000 is used for digital delay, providing delay according to signal specified time (max. of 1024 seconds).
The DRAM for external connection is 256Kbit.
The Digital Delay and Equalizer circuitry are controlled by latched data of IC25 (74HC174) which is connected to the DATA BUS from the main circuit board KLM-1032 CPU. This control is carried out via FET switches F1 and F3 ON/OFF control of Digital Delay parameter settings, EQ parameter setting and Digital Delay circuitry.

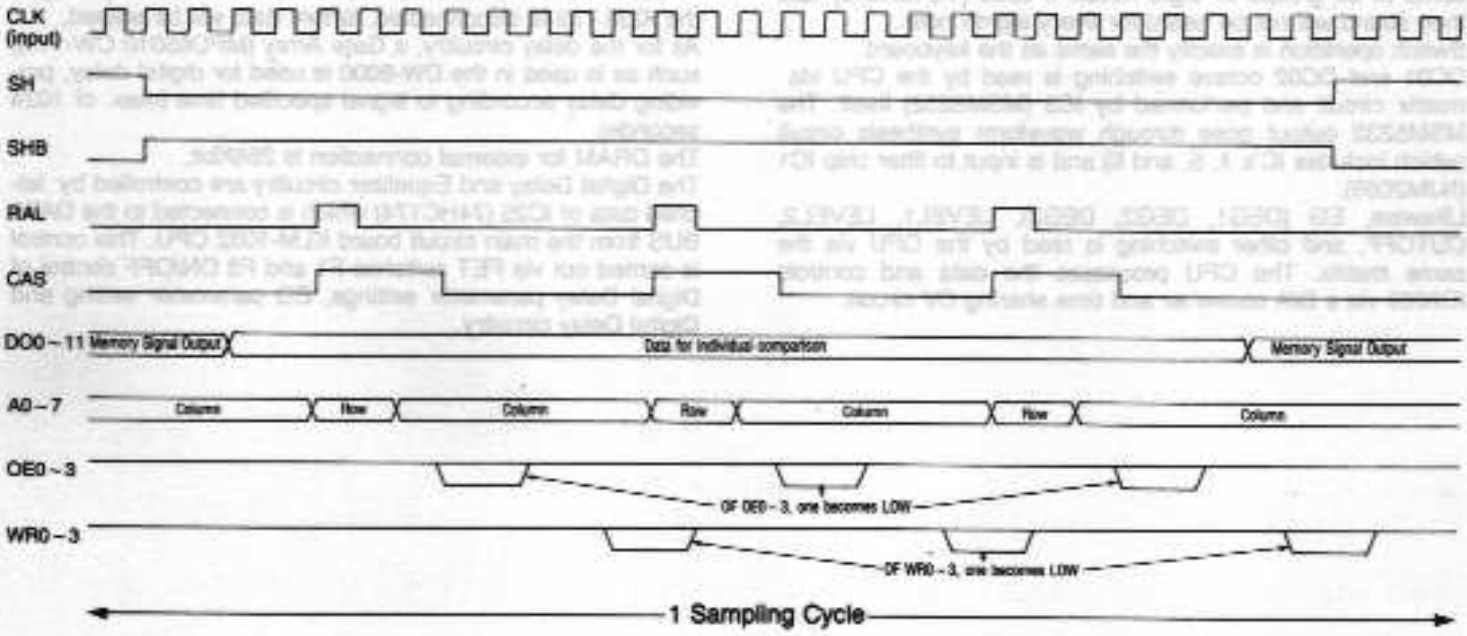
3. μPD 65010 CW-113 SPECIFICATIONS

TERMINAL NAMES

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
1	HOLD	I	23	DO8	O	44	A0	O
2	RST1	I	24	DO7	O	45	WR0	O
3	RST2	I	25	DO6	O	46	IO3	I/O
4	SPON	I	26	DO5	O	47	IO2	I/O
5	STRT	I	27	DO4	O	48	CAS	O
6	X1	I	28	CO3	O	49	OE0	O
7	PRSR	I	29	DO2	O	50	IO1	I/O
8	256K	I	30	DO1	O	51	IO4	I/O
9	D9	I	31	DO0	O	52	OE1	O
10	D8	I	32	GND	0V	53	OE2	O
11	TCO	O	33	WR3	O	54	OE3	O
12	TE13	I	34	WR2	O	55	D0	I
13	TMOD	I	35	WR1	O	56	D1	I
14	MTEN	I	36	A7	O	57	D2	I
15	MUTB	O	37	A4	O	58	D3	I
16	MUTE	O	38	A3	O	59	D4	I
17	SHB	O	39	A5	O	60	D5	I
18	SH	O	40	A2	O	61	D6	I
19	DATA	I	41	A6	O	62	D7	I
20	DO11	O	42	A1	O	63	CLK	I
21	DO10	O	43	RAS	O	64	VDD	+5V
22	DO9	O						

PIN CONFIGURATION

OUTPUT TERMINAL TIMING CHART



NOTE: The timing shown is for normal operation, with ×1 input being low.

8. CHECK AND ADJUSTMENT PROCEDURE

ADJUSTMENT PROCEDURE

Caution:
This product has been thoroughly abjusted at the factory before shipment. Therefore do not abjust anything other than those VRs required for servicing.
BEFORE making any calibration abjustments, Be sure that test data is loaded into POLY-800.
The following setting chart shows the program data used for servece testing. After inputting the data, save it on tape for future time saving convenience.

PROGRAM no. 11 (noise level):

Parameter:	17	18	31	32	33	35	37	61	62	63	64	65	66	83	84
Value:	0	1	99	0	0	0	15	0	0	31	0	31	0	0	0

PROGRAM no. 21 (master oscillator):

Parameter:	11	12	13	14	15	16	17	18	31	32	33	35	38	41	42	43	44	45	46	83	84
Value:	2	2	1	0	0	0	30	1	60	0	0	0	0	0	0	31	0	31	0	0	0

PROGRAM no. 13 (cut off):

Parameter:	11	12	13	14	15	16	17	18	31	32	33	35	37	41	42	43	44	45	46	83	84
Value:	2	2	1	0	0	0	31	1	12	12	2	0	0	0	0	31	0	31	0	0	0

PROGRAM no. 14 (resonance):

Parameter:	11	12	13	14	15	16	17	18	31	32	33	35	37	41	42	43	44	45	46	81	82	83	84
Value:	2	2	1	0	0	0	31	1	99	15	0	0	0	0	0	31	0	31	0	15	0	0	0

PROGRAM no. 15 (delay 1):

Parameter:	11	12	13	14	15	16	17	18	31	32	33	35	37	41	42	43	44	45	46	61	71	72	73	74	75	76	77	81	82	83	84	85	86	81	88
Value:	1	1	1	1	1	1	31	1	99	0	0	1	0	0	0	7	0	0	0	0	50	15	0	0	15	0	0	0	0	0	0	2	1	1	0

PROGRAM no. 16 (delay 2):

Parameter:	11	12	13	14	15	16	17	18	31	32	33	35	37	41	42	43	44	45	46	61	71	72	73	74	75	76	77	81	82	83	84	85	86	81	88
Value:	1	1	1	1	1	1	31	1	99	0	0	1	0	0	0	7	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	2	1	1	0

1. Power supply circuit (KLM-1032)

Be sure that the specified AC adapter is used: 9V, 300mA,

1) +5V check and adjustment:
Use a DVM (digital voltmeter) to check KLM-596 connector CN6 Pin 6 and confirm +5V (±0.005V). Adjust VR1 if necessary.

2) −5V check:
Use a DVM to check KLM-596 connector CN6 Pin 8 and confirm −5V (within −4.7V ~ −5.7V)

2. D/A converter check and adjustment (KLM-1032)

With joystick bend control at center position: (BEND INT MAX) connect DVM to KLM-596 IC10 (TL062) Pin 7 and confirm 1.986V ±0.005V. Adjust VR4 if necessary.
Reference data:
3.990V for an upward pitch bend and
0.020V for a downward pitch bend.

Note:
Adjustment is easiest in the joystick circuit although the idea is to obtain a 4V ±0.004V output from IC 38 (TL062) by adjusting the D/A converter when IC 81C55 port A output is all high.

3. Noise level check and adjustment: (KLM-1032)

1) Select program no. 11.

2) Depress C3 key and set to HOLD.

3) Connect on oscilloscope to KLM-596 CN6A 3 pin and confirm noise level of 0.3Vp-p (±20%).

4) Adjust VR3 if necessary.

4. Master oscillator check and adjustment: (KLM-1032)

Set tune knob to center and bend intensity to maximum. Connect AT-12 to line out jack.

1) Select program no. 12.

2) Play C3 key and set to HOLD.

3) Confirm AT-12 indication of — 1 OCT, C, 0 cent. If necessary, abjust coil KL-003.

4) Next, move joystick to maximum upward pitch bend position and confirm AT-12 reading of — 1 OCT, G, +35 cents. Adjust KLM-601 VR2 if necessary.

5) At maximum joystick downward pitch bend, AT-12 indication should be −2 OCT, −35 cents. Adjust KLM-601 VR1 if necessary.

- VR3 is a semi-fixed resistor to fix range of tune VR on front panel.
  Confirm +40 ~ +70 cents when tune VR is at # max position.
- Confirm −40 ~ −70 cents when tune VR is at b max position.
  If necessary, Adjust VR3.

5. Cutoff check and adjustment: (KLM-1032)

1) Select program no. 13.

2) Play C3 and set to HOLD.

3) Connect on oscilloscope to CN6A pin 3 and observe waveform as in figure 1.

4) Adjust VR2 to obtain maximum waveform amplitude.

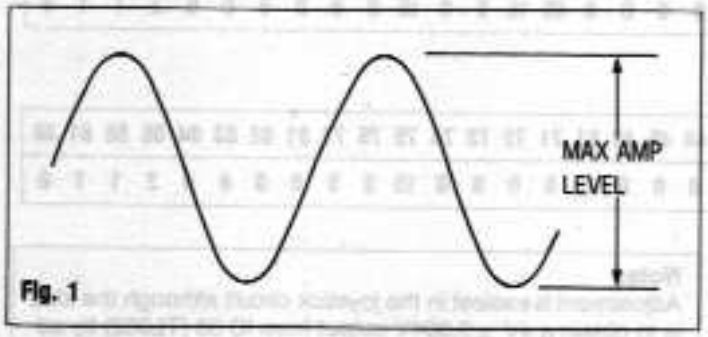


Fig. 1

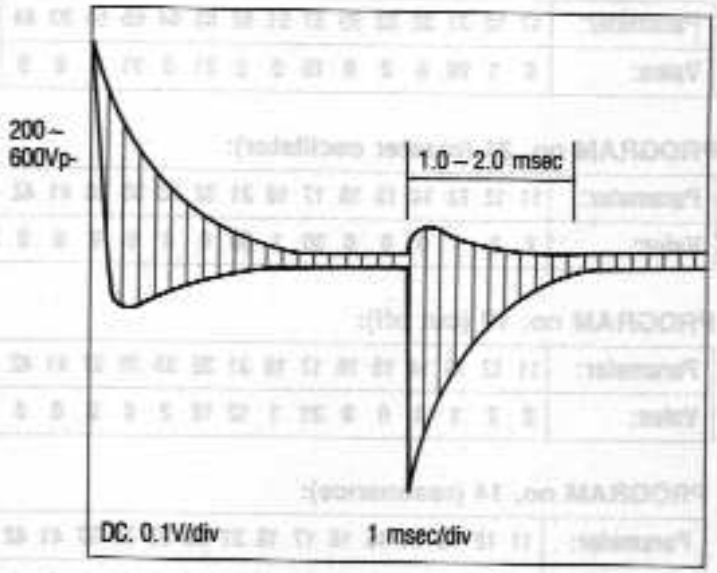
6. Resonance check and adjustment: (KLM-1032)

1) Select program no. 14.

2) Play C3 and set to HOLD.

3) Confirm to oscillation and confirm that waveform is as shown in figure 2.

4) Abjust VR5 if necessary to prevent oscillation or to correct waveform deviation from figure 2 example.



7. S/H CLOCK check and adjustment

1. S/H CLOCK Verification, Adjustment

1) Connect a frequency counter to TEST POINT 3 (TP3).

2) Check that the frequency counter displays 20kHz ±0.5kHz.

3) Abjust VR3 if necessary.

NOTE:
Waveforms on the oscilloscope are as follows; (Fig-1)

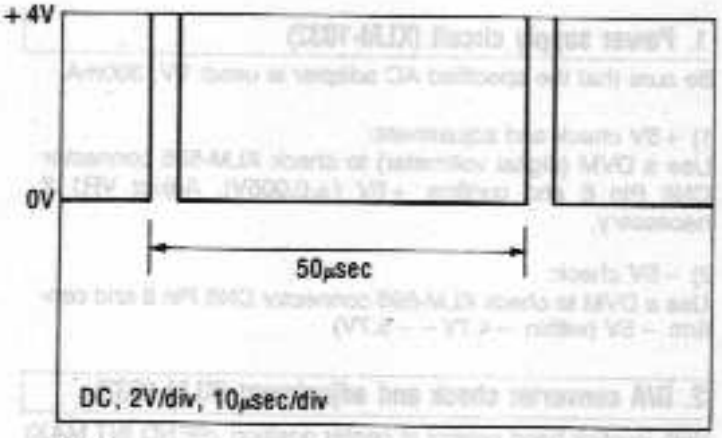


Fig-1

2. FEEDBACK TIME Verification, Adjustment

1) Select program No. 15.

2) Connect on oscilloscope (AC, 50mV/div, 0.1 sec/div) to TP1.

3) Play C3 key, and check that the envelope of the waveform (from peak of waveform to decay) is 600msec ±50msec. (Fig-2)

4) Adjust VR 1 if necessary

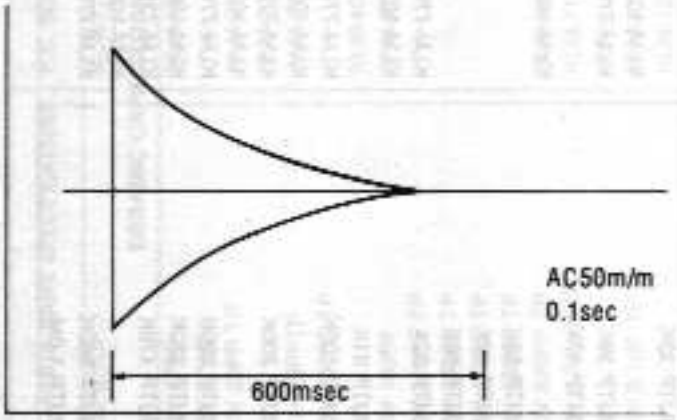


Fig-2

3. ANALOG COMPANDER NE572 Verification, Adjustment

1) Select program No. 16.

2) Connect on oscilloscope (AC 50mV/div, 0.1 sec/div) to TP1. (Connect ground to TP2)

3) Play C3 key, and check on the oscilloscope that visible waveforms are formed which are uniform in size and shape.

Note:
Although this can be abjusted via VR2, because it is fixed at a fully couterclockwise position, so it should not be turned.