CMI-35 2.14
Digital Mother Board

Terminology
WP - Waveform Processor CMI-33
CS - Channel Support Card CMI-32
WRAM - Waveform RAM CMI-39
RAM - System RAM Q256

Introduction

All of the digital CMI modules described in chapters 2.2 to 2.13 of this manual, plug directly into 78 pin edge connectors mounted on the CMI digital motherboard CMI-35. This is in turn mounted on the rear of the CMI card cage. The motherboard is the means by which all logic signals and power supplies are routed between the plug-in modules. This section specifies each of these signals for each module, starting from the left.

All modules are "double sided" so require two columns of pins on each connector. "Side A" refers to the wiring side of a plug-in module which corresponds to the left hand column of pins on the motherboard when viewed from the front of the card cage. Conversely, "Side B" refers to the component side of the module and connects to the right hand column of pins on the edge connector.

Pin numbers not included in the following lists are not used, and have no connection on the motherboard. Signals which are listed but have "N/C" entered as the source or destination are those which have been connected to edge connector fingers but have no connections leading to or from the corresponding pins on the motherboard.

A pin specified as an input ("I/P") will have the Source module which drives that input entered in the Source/Destinations column. Conversely an output ("O/P") will have the Destination or driven module entered in the Source/Destinations column.

Active-low signals are indicated by overlining. All other signals are active-high. Where different names have been used for one signal going between various modules, the Signal Name column contains the name for the module of the current section, and the alternative name is enclosed in brackets in the Source/Destination column.

This document refers to the CMI-35 Rev. 3 motherboard.

General Description

The Series III CMI contains two entirely independent busses, and this is reflected in the layout of the CMI-35 motherboard. The first buss is the 2MHz dual-6809 processor buss, or CPU buss. It extends from the slot-27 end of the board on which the Q-777 SCSI controller resides up to slot 16, the Channel Support slot. Part of the CPU buss then extends further to slot 8 which is occupied by Channel 8. The only cards which have no connections at all to the CPU buss are the Waveform RAM cards. The CPU buss comprises 16 bits of address, 8 bits of data plus the system reset signal, CPU timing signals, DMA arbitration, daisy chain, and mapping signals, Peripheral Enable, Interrupts, and a few control signals.

The second buss in the system is the 3.3MHz Waveform Bus which extends from the slot-1 end of the CMI-35 board up to the Waveform Processor on slot 17. It comprises 23 address bits, 16 data bits, two data strobes, Channel card timing signals, a 17-MHz Master Oscillator differential pair, a 10MHz Processor Clock differential pair, a 3.3MHz buss clock, Channel Select lines, refresh controls, and Channel arbitration signals.

CPU Bus Signals

The following connections are common to all slots on the CPU buss and travel from slot 27 to slot 8, except that the signals on pins 9A to 17A stop at slot 15. The buss lines are arranged in a ground shield interleave pattern which provides protection against electromagnetic noise pickup and cross-talk between adjacent signal tracks. Not all modules use all the busssed signals.

Side A

Pin	Signal Name	Function	Source
42	SYRES	System reset	Q133
41	ADD2	P2 address on buss[1]	Q209
40	ADD1	P1 address on buss[1]	Q209
39	P2ø2	P2 phase 2 reference	Q209
38	P1ø2	P1 phase 1 reference	Q209
37	$\overline{RA}$	Row address mux signal	Q209
36	$\overline{CA}$	Column address mux sig.	Q209
35	$\overline{RAS}$	Row address strobe	Q209
34	$\overline{CAS}$	Column address strobe	Q209
33-26	D0-D7	Data Buss	Various
25-18	MA0-MA7	Address Buss, upper half	Various
17-10	MA8-MA15	Address Buss, lower half[2]	Various
17	ADD2	P2 address on buss[1]	Q209
16	ADD1	P1 address on buss[1]	Q209
9	VMA	Valid Memory Address[2]	Various
8	R/W	Read/write	Various
7	Key	Socket index key	
6	+12V	+12V supply rail	
3	-12V	-12V supply rail	
2,1	GND	Ground rail	

Side B

Pin	Signal Name	Function	Source
44-46	GND	Ground rail	
42-1	GND	Ground shielding pattern	
5,4,2,1	GND	Ground rail	

Notes
1. The P2ø2 and P1ø2 signals are on pins 39A and 38A respectively of slots 27 to 16, then pins 17A and 16A of slots 15 to 8.
2. The lower half of the address bus and the VMA signal only go from slots 26 to 16, and do not go to the Channels card slots.

Waveform Bus Signals

The following signals are common to all slots on the Waveform Bus and travel from slot 1 to slot 15. The Channel Support Card on slot 16 also connects to the Waveform Bus but some connections are different Not all the modules use all the signals.

Side A

Pin	Signal Name	Function	Source
67	$\overline{\text{BLOCKSEL}}$	All-channel select[1]	CS
66	$\overline{\text{WUDS}}$	Waveform Upper Data Strobe	WP
65	WLDS	Waveform Lower Data Strobe	WP
64-57	WA8-WA1	Waveform Address lower byte	Various
56-49	WD7-WD0	Waveform Data lower byte	Various
48	CHANTICK	Chan. processor interrupt clock[1]	CS
47	DRAS	Delayed RAS for channel RAM[1]	CS
46	2E	2MHz E clock for chan. proc.[1]	CS
45	2Q	2MHz Q clock for chan. proc.[1]	CS
44	PCLK	10MHz clock for WP and chans[2]	CS
43	$\overline{\text{PCLK}}$	10MHz clock for WP and chans[2]	CS
42	$\overline{\text{SYRES}}$	System Reset from CPU	CCC
39	MOSC	Master Oscillator[3]	CS
38	$\overline{\text{MOSC}}$	Master Oscillator[3]	CS

Side B

Signal Pin	Name	Function	Source
75	SCLK	3.3MHz Waveform Bus clock[4]	CS
74	TSTAKEN	Time Slice Taken	Channels
73	8BIT	8-bit mode select	Channels, WP
72	WAS	Waveform Address Strobe	WP
71	WRW	Waveform Read/Write	WP
70-56	WA23-WA9	Waveform Address high bits	Channels, WP
55-48	WD15-WD8	Waveform Data high byte	WP, WRAM
47	REFRESH	Channel refresh strobe	CS
46-44	GND	Ground Rail	
5,4,2,1	GND	Ground Rail	

Notes

1. Slots 16 to 8 only
2. Differential pair, slots 17 to 8 only
3. MOSC and MOSC are the differential pair which drive the 17Mhz Master Oscillator used as the pitch reference by all channel cards. It is generated on the Channel Support Card, slot 16 onto pins 78B and 77B. These pins connect to link connector holes "A" and "B" near the top of slot 16 the pair of signals then goes via a twisted pair flying connection to another two link connector holes marked "A" and "B" near the middle of slot 15. The latter holes connect to pins 39A and 38A of slot 15 and the MOSC signal are then bussed along all channel card slots.
4. SCLK is a rectangular wave clock: 100nS high, 200nS low.

Slots 1 to 7: Waveform RAM

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
67	WREF	Waveform Refresh	I/P	WP
66-49	see Sec. X.3			

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Last Time Slice out	I/P	Ch. 7
75-48	see Sec. X.3			

Slot 8: Channel 8
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	$\overline{SO}$	Time Slice Out	O/P	WRAMs (TSLICE)
68	$\overline{CHSEL8}$	Channel 8 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	$\overline{TSLICE}$	Time Slice In	I/P	Ch. 7 (SO)
17	$\overline{CHINT}$	Channel interrupt	O/P	Q133 (IL21)

Slot 9: Channel 7
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	$\overline{SO}$	Time Slice Out	O/P	Ch. 8 (TSLICE)
69	$\overline{CHSEL7}$	Channel 7 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	$\overline{TSLICE}$	Time Slice In	I/P	Ch. 6 (SO)
17	$\overline{CHINT}$	Channel interrupt	O/P	Q133 (IL21)

Slot 10: Channel 6
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 7 (TSLICE)
68	CHSEL6	Channel 6 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Time Slice In	I/P	Ch. 5 (SO)
17	CHINT	Channel interrupt	O/P	Q133 (IL21)

Slot 11: Channel 5
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 6 (TSLICE)
68	CHSEL5	Channel 5 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Time Slice In	I/P	Ch. 4 (SO)
17	CHINT	Channel interrupt	O/P	Q133 (IL21)

Slot 12: Channel 4
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 5 (TSLICE)
68	CHSEL4	Channel 4 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Time Slice In	I/P	Ch. 3 (SO)
17	CHINT	Channel interrupt	O/P	Q133 (IL21)

Slot 13: Channel 3
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 4 (TSLICE)
68	$\overline{\text{CHSEL3}}$	Channel 3 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Time Slice In	I/P	Ch. 2 (SO)
17	$\overline{\text{CHINT}}$	Channel interrupt	O/P	Q133 (IL21)

Slot 14: Channel 2
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 3 (TSLICE)
68	$\overline{\text{CHSEL2}}$	Channel 2 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	Time Slice In	I/P	Ch. 1 (SO)
17	$\overline{\text{CHINT}}$	Channel interrupt	O/P	Q133 (IL21)

Slot 15: Channel 1
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	SO	Time Slice Out	O/P	Ch. 2 (TSLICE)
68	$\overline{\text{CHSEL1}}$	Channel 1 select	I/P	CS

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
77	ADCLK	A/D Convertor clock	O/P	WP
76	TSLICE	Time Slice In	I/P	CS
17	$\overline{\text{CHINT}}$	Channel interrupt	O/P	Q133 (IL21)

Slot 16: Channel Support Card
Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	TSLICE	First Time Slice	O/P	Ch. 1
75	$\overline{\text{CHSEL1}}$	Channel 1 select	O/P	Ch. 1
74	$\overline{\text{CHSEL2}}$	Channel 2 select	O/P	Ch. 2
73	$\overline{\text{CHSEL3}}$	Channel 3 select	O/P	Ch. 3
72	$\overline{\text{CHSEL4}}$	Channel 4 select	O/P	Ch. 4
71	$\overline{\text{CHSEL5}}$	Channel 5 select	O/P	Ch. 5
70	$\overline{\text{CHSEL6}}$	Channel 6 select	O/P	Ch. 6
69	$\overline{\text{CHSEL7}}$	Channel 7 select	O/P	Ch. 7
68	$\overline{\text{CHSEL8}}$	Channel 8 select	O/P	Ch. 8
66	REFEN	Refresh enable	I/P	Q133 ($\overline{\text{ENL1}}$)
65	ACK1	P1 DMA Acknowledge	I/P	Q209

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
78	MOSC	Master Oscillator[1]	O/P	Channels
77	$\overline{\text{MOSC}}$	Master Oscillator[1]	O/P	Channels
76	$\overline{\text{TIMINT}}$	Timer Interrupt	O/P	Q133 (IL11)
43	PENB	Peripheral Enable	I/P	RAM, Card 0

Notes
1. MOSC and $\overline{\text{MOSC}}$ are the differential pair which drive the 17MHz Master Oscillator used as the pitch reference by all channel cards. It is generated on the Channel Support Card, slot 16 onto pins 78B and 77B. These pins connect to link connector holes "A" and "B" near the top of slot 16 the pair of signals then goes via a twisted pair flying connection to another two link connector holes marked "A" and "B" near the middle of slot 15. The latter holes connect to pins 39A and 38A of slot 15 and the MOSC signal are then bussed along all channel card slots.

Slot 17: Waveform Processor

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	$\overline{\text{P2DMAC}}$	P2 DMA Claim	O/P	RAMs (DMAC24)
75	$\overline{\text{P1DMAC}}$	P1 DMA Claim	O/P	RAMs (DMAC12)
71	WREF	Waveform Refresh	O/P	WRAMs
70	$\overline{\text{ETL2}}$	P2 Enable This Level	I/P	SMIDI ($\overline{\text{ENL2}}$)
69	$\overline{\text{ENL2}}$	P2 Enable Next Level	O/P	SCSI ($\overline{\text{ETL}}$)
68	ETL1	P1 Enable This Level	I/P	SMIDI ($\overline{\text{ENL1}}$)
67	ENL1	P1 Enable Next Level	O/P	N/C
48	ACK2	P2 DMA Acknowledge	I/P	Q209
47	$\overline{\text{RDMA2}}$	P2 Request DMA	O/P	Q209
46	ACK1	P1 DMA Ackknowledge	I/P	Q209
45	$\overline{\text{RDMA1}}$	P1 Request DMA	O/P	Q209

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	ADCLK	AD Convertor Clock	I/P	Ch. 1
43	$\overline{\text{FCXX}}$	Control latch select	I/P	Q133

Slot 18: General Interface Card CMI-28

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78,77	+5V	+5V Logic supply		
76	P2DMAC	P2 DMA claim	O/P	RAMs (DMAC24)
75	P1DMAC	P1 DMA claim	O/P	RAMs (DMAC11)
70	ETL2	P2 DMA Enable This Level	I/P	QFC9 (ENL)
69	ENL2	P2 DMA Enable Next Level	O/P	WP (ETL2)
68	ETL1	P1 DMA Enable This Level	I/P	Q133 (ENL1)
67	ENL1	P1 DMA Enable Next Level	O/P	WP (ETL1)
66	MIDINT	MIDI IRQ	O/P	Q133 (IL01)
65	SMPTEINT	SMPTE IRQ	O/P	Q133 (IL31)
64	FCXX	Control latch select	I/P	Q133
48	ACK2	P2 DMA Acknowledge	I/P	Q209
47	RDMA2	P2 DMA Request	O/P	Q209
46	ACK1	P1 DMA Acknowledge	I/P	Q209
45	RDMA1	P1 DMA Request	O/P	Q209

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
69	MIDINT	MIDI IRQ	O/P	N/C
68	SMIDINT	SMPTE IRQ	O/P	N/C
67	FCXX	Port select	I/P	N/C

The B-side signals on pins 67-69 are duplicates of the corresponding signals on side A, and are only used when a CMI-28 module is installed in a Series I machine upgraded to Series IIX.

Slot 19: Spare

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78,77	+5V	+5V Logic supply		
54	$\overline{FCXX}$	Port select	I/P	Q133
46	$\overline{IRQ}$	Interrupt	O/P	Q133(IL41)

Slots 20,21: System RAM Q256

One Q256 module must be installed in slot 21. This is referred to as Card 0 and must have zero set up on the card select DIP switch on the board (see Q256 description). A second Q256 module may be installed in slot 20, and should be switched as Card 1.

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	$\overline{BE1}$	P1 E signal (unused)	I/P	Q209
75	$\overline{DMAC11}$	P1 DMA claim level 1	I/P	Gen. I/F ($\overline{P1DMAC}$)
74	$\overline{DMAC12}$	P1 DMA claim level 2	I/P	WP ($\overline{P1DMAC}$)
73	$\overline{DMAC13}$	P1 DMA claim level 3	I/P	N/C
72	$\overline{DMAC14}$	P1 DMA claim level 4	I/P	N/C
71	$\overline{DMAC21}$	P2 DMA claim level 1	I/P	Floppy ($\overline{DMACLM}$)
70	$\overline{DMAC22}$	P2 DMA claim level 2	I/P	H. Disk ($\overline{DMACLM}$)
69	$\overline{DMAC23}$	P2 DMA claim level 3	I/P	WP ($\overline{P2DMAC}$)
68	$\overline{DMAC24}$	P2 DMA claim level 4	I/P	Gen. I/F ($\overline{P2DMAC}$)
65	$\overline{RAMINH}$	System RAM Inhibit	I/P	Graphics ($\overline{VRAMSEL}$)
64	$\overline{FCXX}$	Port select (Mapsel RAM)	I/P	Q133
63	A/$\overline{B2}$	P2 System/User State	I/P	Q209
62	A/$\overline{B1}$	P1 System/User State	I/P	Q209
52	PENBIN	Peripheral Enable In[1]	I/P	RAM, Card 0 (PENBOUT)
51	PENBOUT	Peripheral Enable Out[1]	O/P	Various
50	VRAMEN	Video RAM Enable[2]	O/P	Graphics
48	REF	Refresh cycle	I/P	Q133
46	PERRINT	Parity Error IRQ	O/P	Q133 (IL02)

Notes

1. The PENB (Peripheral Enable) signal is driven by the PENBOUT pin 52A of RAM card 0 only, in slot 21. PENB goes to all cards which act as peripherals on the CPU bus, including PENBIN of both RAM cards on pin 51A. The main RAM is not a peripheral, but the MAPSEL and MAPRAM are (see Q256 documentation). PENBOUT of card 1 is N/C.
2. The VRAMEN output from RAM card 0 only goes to the Graphics card. VRAMEN of card 1 is N/C.

Slot 22: Q014 4-Port ACIA Module (Optional)

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
66	ENB	Peripheral Enable	I/P	RAM (PENBOUT)
65-58	IRQ0-7	Individual ACIA IRQs	O/P	N/C
57	IRQ8	Combined IRQ	O/P	Q133 (IL62)
56-53	AS6-AS9	Address select	I/P	N/C

Slot 23: Processor Control Module Q133

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	IL32	P2 level 3 IRQ	I/P	Q209 (IPI2)
75	IL22	P2 level 2 IRQ	I/P	N/C
74	IL12	P2 level 1 IRQ	I/P	Graphics (RINT)
73	IL02	P2 level 0 IRQ	I/P	Q133 (RTCINT) & RAM (PERRINT)
72	IL31	P1 level 3 IRQ	I/P	Q209 (IPI1) & GIF (SMPTEINT)
71	IL21	P1 level 2 IRQ	I/P	All Chs (CHINTX)
70	IL11	P1 level 1 IRQ	I/P	Ch. Supp (TIMINT)
69	IL01	P1 level 0 IRQ	I/P	GIF (MIDINT)
68	ILS2	P2 PICU latch strobe	I/P	Q209
67-64	IA42-IA12	P2 intrpt vector addr.	O/P	Q209
63	IRQ2	P2 interrupt request	O/P	Q209
62	ILS1	P1 PICU latch strobe	I/P	Q209
61-58	IA41-IA11	P1 intrpt vector addr.	O/P	Q209
57	IRQ1	P1 interrupt request	O/P	Q209
56	NMI2	P2 NMI request	O/P	Q209
55	NMI1	P1 NMI request	O/P	Q209
54	RES2	P2 restart	O/P	Q209
53	HLT2	P2 HALT	O/P	Q209
52	RES1	P1 restart	O/P	Q209
51	HLT1	P1 HALT	O/P	Q209
50	W2	P2 halt acknowledge	I/P	Q209
49	W1	P1 halt acknowledge	I/P	Q209
48	REF	Refresh cycle	O/P	RAM
47	PENB	Peripheral enable	I/P	RAM (PENBOUT)
46	ACK1	Refresh acknowledge	I/P	Q209
45	REQ1	Refresh cycle request	O/P	Q209
44	ROMEN	Restart ROM enable	I/P	Q209

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	IL72	P2 level 7 IRQ	I/P	QFC9, SCSI ($\overline{\text{IRQD}}$)
75	IL62	P2 level 6 IRQ	I/P	Q133 (ACINT) & Q014 ($\overline{\text{IRQ8}}$)
74	IL52	P2 level 5 IRQ	I/P	Graphics ($\overline{\text{PENINT}}$)
73	IL42	P2 level 4 IRQ	I/P	Graphics ($\overline{\text{TOUCHINT}}$)
72	IL71	P1 level 7 IRQ	I/P	N/C
71	IL61	P1 level 6 IRQ	I/P	N/C
70	IL51	P1 level 5 IRQ	I/P	N/C
69	IL41	P1 level 4 IRQ	I/P	Spare ($\overline{\text{IRQ}}$)
68	$\overline{\text{ACINT}}$	Keyboard ACIA IRQ	O/P	Q133 (IL62)
67	$\overline{\text{IRQPA}}$	User PIA IRQ A	O/P	N/C
66	$\overline{\text{IRQPB}}$	User PIA IRQ B	O/P	N/C
65	$\overline{\text{ENL1}}$	P1 DMA Enable Next Level	O/P	GIF ($\overline{\text{ETL1}}$) & Ch Supp (REFEN)
64	$\overline{\text{FCXX}}$	Ports access	O/P	Various
63	$\overline{\text{RTCINT}}$	Real time clock intrpt	O/P	Q133 (IL02)
62,61		Current loop TX	O/P	N/C
60	$\overline{\text{FXXX}}$	FXXX address range decode	O/P	N/C

Slot 24: Central Processor Module Q209

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	BE1	P1 "E" signal	O/P	RAM, Spare
75	$\overline{\text{FIRQ2}}$	P2 Fast IRQ	I/P	N/C
74	$\overline{\text{FIRQ1}}$	P1 Fast IRQ	I/P	N/C
73	$\overline{\text{IPI2}}$	P2 Interprocessor Intrpt	O/P	Q133 (IL32)
72	$\overline{\text{IPI1}}$	P1 Interprocessor Intrpt	O/P	Q133 (IL31)
71	$\overline{\text{FCXX}}$	Port select	I/P	Q133
70	A/$\overline{\text{B}}$2	P2 System/User state	O/P	RAM
69	A/$\overline{\text{B}}$1	P1 System/User state	O/P	RAM
68	ILS2	P2 PICU latch strobe	O/P	Q133
67-64	IA42-IA12	P2 intrpt vector addr.	I/P	Q133
63	$\overline{\text{IRQ2}}$	P2 interrupt request	I/P	Q133
62	ILS1	P1 PICU latch strobe	O/P	Q133
61-58	IA41-IA11	P1 intrpt vector addr.	I/P	Q133
57	$\overline{\text{IRQ1}}$	P1 interrupt request	I/P	Q133
56	$\overline{\text{NMI2}}$	P2 NMI request	I/P	Q133
55	$\overline{\text{NMI1}}$	P1 NMI request	I/P	Q133
54	$\overline{\text{RES2}}$	P2 restart	I/P	Q133
53	$\overline{\text{HLT2}}$	P2 HALT	I/P	Q133
52	$\overline{\text{RES1}}$	P1 restart	I/P	Q133
51	$\overline{\text{HLT1}}$	P1 HALT	I/P	Q133
50	W2	P2 in wait state (BA)	O/P	Q133
49	W1	P1 in wait state (BA)	O/P	Q133
48	ACK2	P2 DMA acknowledge	O/P	QFC9, SCSI, WP, GIF
47	$\overline{\text{REQ2}}$	P2 DMA request	I/P	QFC9, SCSI, WP, GIF
46	$\overline{\text{ACK1}}$	Refresh cycle grant	O/P	Q133, WP, GIF, CS
45	$\overline{\text{REQ1}}$	Refresh cycle request	I/P	Q133, WP, GIF
44	ROMEN	Restart ROM enable	O/P	Q133
43	OSC	Master proc. clock	O/P	N/C

Slot 25: Lightpen/Graphics Interface Q219

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
68	$\overline{\text{RINT}}$	Timer IRQ	O/P	Q133 (IL12)
67	$\overline{\text{PENINT}}$	Light pen hit IRQ	O/P	Q133 (IL52)
66	TOUCHINT	Light pen touch IRQ	O/P	Q133 (IL42)
65	VRAMEN	Video RAM Enable	I/P	RAM Card 0
64	$\overline{\text{FCXX}}$	Port select	I/P	Q133
63	VRAMSEL	Video Ram Select	O/P	RAM ($\overline{\text{RAMINH}}$)

Slot 26: Floppy Disc Controller QFC-9

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
71	$\overline{\text{EDL}}$	Enable Daisy Links	O/P	Floppy $\overline{\text{ETL}}$[1]
70	$\overline{\text{ETL}}$	Enable This Level	I/P	Floppy & SCSI $\overline{\text{EDL}}$[1]
69	$\overline{\text{ENL}}$	Enable Next Level	O/P	GIF ($\overline{\text{ETL}}$)
68	$\overline{\text{DMACLM}}$	DMA claim	O/P	RAM ($\overline{\text{DMAC21}}$)
65	$\overline{\text{PENB}}$	Peripheral Enable	I/P	RAM card 0
63	$\overline{\text{IRQD}}$	Floppy Controller IRQ	O/P	Q133 (IL72)
48	$\overline{\text{ACK2}}$	DMA cycle grant	I/P	Q209
47	$\overline{\text{RDMA}}$	DMA request	O/P	Q209 ($\overline{\text{REQ2}}$)

Slot 27: SCSI Controller Q777

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
72	$\overline{\text{EDL}}$	Enable Daisy Links	O/P	GIF ($\overline{\text{ETL}}$)[2]
71	$\overline{\text{EDL}}$	Enable Daisy Links	O/P	Floppy $\overline{\text{ETL}}$[1]
70	$\overline{\text{ETL}}$	Enable This Level	I/P	WP ($\overline{\text{ENL2}}$)
69	$\overline{\text{ENL}}$	Enable Next Level	O/P	N/C
68	$\overline{\text{DMACLM}}$	DMA claim	O/P	RAM ($\overline{\text{DMAC22}}$)
65	$\overline{\text{PENB}}$	Peripheral Enable	I/P	RAM card 0
63	$\overline{\text{IRQD}}$	SCSI Controller IRQ	O/P	Q133 (IL72)
48	$\overline{\text{ACK2}}$	DMA cycle grant	I/P	Q209
47	$\overline{\text{RDMA}}$	DMA request	O/P	Q209 ($\overline{\text{REQ2}}$)

Notes
1. $\overline{\text{EDL}}$ outputs of both QFC-9 and Q777 go to $\overline{\text{ETL}}$ input of QCF-9. Link optioning on the two controller boards determines which output is actually used. QFC-9 output should only be used if no Q777 is installed. See section X.25.
2. Extra $\overline{\text{EDL}}$ output from Q777 bypasses the QFC-9 and goes directly to $\overline{\text{ETL}}$ input of GIF card to allow system to be run without QFC-9 card. Currently pin 72A of Q777 is not driven. See section X.25.

Series III CPU Interrupt Level Assignments

Processor 1

Level	Source(s)		o/c	IRQ input
0	MIDIINT: CMI-28 66A	*	y	IL01: DBG 69A
1	TIMINT: Ch. Supp. 76B	*	y	IL11: DBG 70A
2	CHINT: All channels 10B-17B		y	IL21: DBG 71A
3	P1 IPI: CPU 72A	*	y	IL31: DBG 72A
	SMPTE: CMI-28 65A		y	
4	AIC: AIC 46A	*	y	IL41: DBG 69B
5	-			IL51: DBG 70B
6	-			IL61: DBG 71B
7	-			IL71: DBG 72B

Processor 2

Level	Source(s)		o/c	IRQ input
0	RTCINT: DBG 63B		y	IL02: DBG 73A
	PERRINT: Q256 46A		y	
1	LPEN timer: Q219 68A		y	IL12: DBG 74A
2	-			IL22: DBG 75A
3	P2 IPI: CPU 73A		y	IL32: DBG 76A
4	TOUCHINT: Q219 66A		y	IL42: DBG 73B
5	PEN INT: Q219 67A		y	IL52: DBG 74B
6	Keyboard ACIA: DBG 68B	*	y	IL62: DBG 75B
	ACIAs: Q014 57A		y	
7	DISKS: QFC-9, Q077, 63A		y	IL72: DBG 76B

Notes
1) * indicates departure from or addition to Series II assignments
2) "y" in the o/c column indicates IRQ outputs which are open collector and can therefore be wired in paralled with other IRQs on the same level if desired.
3) Source and IRQ input columns give the name of the interrupt followed by the card and edge connector pin number.
4) There is no second P1 interrupt control unit in Series III as there was on the Master Card in Series II. Hence the wiring together of all Channel interrupts.

Series III DMA Daisy Chain Assignments

Modification history
Rev 3: Provision for $\overline{EDL}$ from either Q777 or QFC-9 to QFC -9 $\overline{ETL}$, and provision for $\overline{EDL}$ direct from Q777 to CMI-28.

Arbitration between the various devices which can access the CPU buss via DMA (cycle-stealing Direct Memory Access) is achieved by a daisy chain. At present the Series III daisy chains are prioritised as follows:

P1: 1. System RAM Refresh (Q133) ($\overline{EDL}$ generated internally)
2. General Interface Card (CMI-28)
3. Waveform Processor (CMI-33)

P2: 0. EDL from either Q777 or QFC-9
1. Floppy controller (QFC-9)
2. General Interface Card (CMI-28)
3. Waveform Processor (CMI-33)
4. SCSI Controller (Q777)

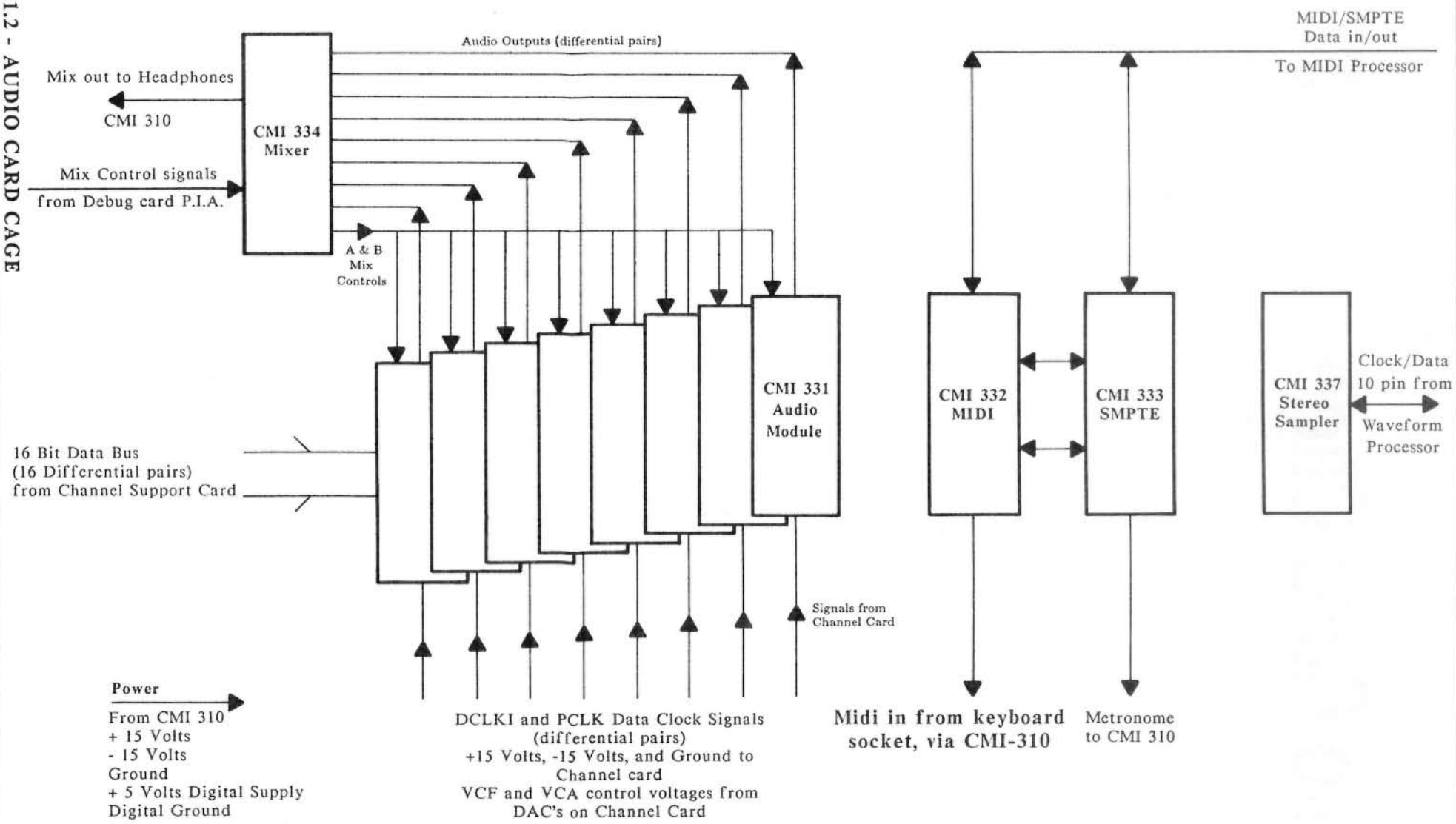
Note that for a given DMA device to work, all higher priority devices must be present in the system or the daisy chain signals for an absent device jumpered on the motherboard. The only exception to this is the bypass link from 72A of the Q777 slot ($\overline{EDL}$) to the GIF $\overline{ETL}$ which allows the system to be run without a QFC-9 simply by linking 71A and 72A on the Q777 board.

The Q256 DMA Channels are assigned as follows:

P1:	Ch 1 SMPTE/MIDI Processor	FC4C
	Ch 2 Waveform Processor	FC4D
	Ch 3 Unused	FC4E
	Ch 4 Unused	FC4F
P2:	Ch 1 Floppy controller	FC44
	Ch 2 SCSI controller	FC45
	Ch 3 Waveform Processor	FC46
	Ch 4 SMPTE/MIDI Processor	FC47

Audio Card Cage 3

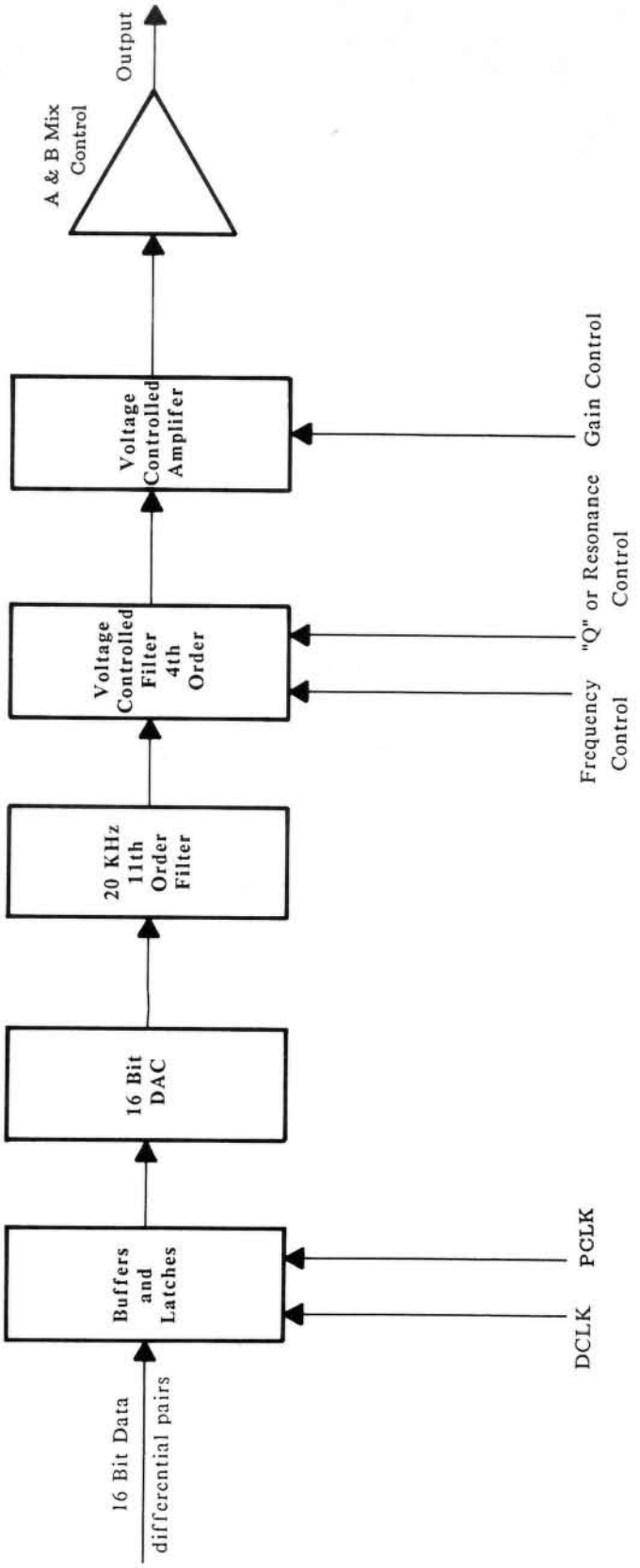
Contents



AUDIO SECTION BLOCK DIAGRAM

(Boards plugged in to CMI 335 Audio Motherboard)

CMI-331 3.2
Audio Module



AUDIO MODULE BLOCK DIAGRAM

1/2 of CMI 331

Terminology
WP: Waveform Processor
WRAM: Waveform Ram (2M-14Mbytes)
CC: Channel Card
CCP: Channel Card Processor
CSC: Channel support Card
CPU: Dual 6809 processor system running OS/9
AM: Audio Module CMI331
AMM: Audio Mixer Module CMI334
AR: Audio Rack Assembly
AMB: Audio MotherBoard CMI335
DAC: Digital to Analog Convertor
WB: Waveform Bus
VCF: Voltage Controlled Filter
Active low signals are preceded by a '/' character.

Introduction

The Audio Module (AM) contains the analog circuitry necessary to filter and control the output from a 16 bit Digital to Analog Convertor (DAC). A typical CMI system contains eight AMs which are located in the rear Audio Rack (AR) slots two through nine. (slots are numbered in Chinese fashion, from right to left looking at the rear of the CMI).
The AM is supplied with all inputs by the Audio MotherBoard (AMB). These include:

Power, which is derived from the CMI310;
Data, which is supplied in differential form from the Channel Support Card (CSC);
Clocks, these are supplied originally from the appropriate Channel Card (CC);
Control Voltages, these also are supplied by the CC;
Control Signals, these are NON-essential controls which may be supplied from the Audio Mixer Module (AMM), see later discussion of control functions for further details.

The only output from the AM is the two audio channels which appear on the rear XLRs and also go to the AMM via the AMB.

Audio Module Structure
(*refer Audio Module Block Diagram*)

As can be seen from the above referenced drawing, sixteen bit data is buffered and latched (by DCLK) on the AM then clocked (by PCLK) into the DAC. The analog output is then fed through an 11th order 20 kHz low pass filter to remove all traces of sampling noise and aliassing. Note that this filter is ineffective for playback rates below approximately 44 kHz, ie when samples are played down pitch. To provide this function for down pitch sounds a fourth order tracking filter is used. The tracking filter also allows some sound effects to be created by altering the cut-off frequency as well as the resonance or 'Q' of the filter. From the tracking filter the audio signal is passed through a voltage controlled amplifier which allows control of the output level, attack and decay of the sound. Finally the signal passes through a switched mixer (under control of the AMM) which is capable of mixing the two audio signals present on the AM to form

form one. This or the separate unmixed signals are buffered and output to the rear panel sockets where the signal is compatible with a 600 ohm balanced line.

Control Structure

Control signals for the AM are supplied from two sources.

1) The CC: this supplies the clocks for latching data from the common data bus and for clocking data into the DAC at the correct rate. Analog signals to drive the Voltage Controlled Filters (VCF) and Voltage Controlled Amplifiers (VCA) are derived from control voltage DACs on the CC.

2) The AMM: this supplies the digital signal to control the two channel mix function as described in section 1.2

The double latching of data into the DAC is necessary to ensure that minimum pitch jitter occurs when the data is strobed in. The first clock is synchronous with the Waveform Bus, giving 4.8uS resolution, while the second is generated by the CC pitch circuitry whose resolution is approx 60nS.

Data Receivers and Power Supplies

(refer schematic CMI331-00)

Digital differential data coming in from the edge connector are buffered and converted into unipolar signals by four MC3486 differential receivers (ICs A-C 13 through 16).

The power supplies are pre-regulated by the CMI310 card which is connected to the Audio Motherboard. Capacitors C1 through C6 decouple these on the AM.

Reference voltages for the DACS and biasing of the analog switch is provided by Q1 & 2 and IC B9, R4 & R5 protect IC B9 in case of short circuit. Note that there is no connection between the digital and analog grounds on this card, therefore if it is powered up while not plugged into the AMB the result may be damage to the DACs. R1, D1&2 help prevent this by limiting drift between these supplies. The AMB has a link between the grounds on the component side between slots 5 and 6.

Output Buffers and Channel Card Inputs

(refer schematic CMI331-01)

This drawing shows the two output driver ICs and the twenty connections from the CC. Note the 6 resistors (100R) and capacitors (1nF) for filtering the analog controls from the CC, these replace six chokes and 0.1uF capacitors from the original rev 1.0 card. If these capacitors are still 0.1uF the Field Change Note upgrade to replace these must be performed since filter oscillation and very high distortion may occur.

Audio output signals are buffered by ICs L2 and L5 (5532) which are capable of directly driving a 600 ohm balanced line. The 33 ohm standoff resistors provide higher tolerance of capacitive loads.

Control Voltages

(refer schematic CMI331-02)

The two filter control sections are shown on the left of the page while on the right the VCA controls are shown.

VCA gain controls are calibrated by RV9 and 10 while RV13 and 14 provide calibration for the +4dBm output level. R121 and R123 are thermistors to compensate for thermal drift of the VCAs. C52 through C55 limit bandwidth and assist with stability as the op amp has a gain of less than 1.

VCF control for the 'A' half of the AM centres around ICs J1,2 and L1. Working backwards, J1,2 pins 1 and 7 supply the control voltages for the four VCAs within the VCF and RN3 (100 ohm) provides isolation between VCA control inputs. R62 and R63 give this stage (pins 1,2 & 3) a gain of 1 while RN4 (1Meg ohm pins 3 and 4) gives a dc offset of approx 460mV so that the filter is set to 20Hz 3dB point with a control voltage of 0V applied.

IC J1,2 (pins 12,13 & 14) has a gain of 6 with R64 giving thermal compenstaion of cut-off frequency. R34 and 43 divide the 0 to 10volt control down to approx 0 to 60 mV.

IC J1,2 (pins 8,9 & 10) is used to cause a variation in control voltage between the 1st and 2nd VCA in each filter stage. This causes an increase in resonance while not changing the passband cut-off point.

The 50k ohm trimmer is used to set the resonance so that flat response is obtained when the control input is set to 0V.

Operation of both halves of the control circuits is identical.

Digital to Analog Convertor and Voltage Controlled Amplifier
(refer schematic CMI331-03 and 04)

Starting from the left, the sixteen bit data is latched from the WB by DCLK into the first set of latches, PCLK clocks the data into the DAC through the second set of latches, the Two current outputs are added and fed via a buffer stage to the 11th order elliptical filter which attenuates unwanted sampling noise to -85dB.

Data is clocked into the first stage of latches (ICs D13,14 &D15,17) by /DCLK through IC A5,6. The pitch clock (/PCLK) (IC A5,6) clocks the data into the second latch stage (ICs E13,14 and E15,17).

The DAC converts this data into 2 current outputs which are converted by IC G12,13 into a voltage of 14Vpeak to peak max at pin 1 of IC G12,13. IC I12 reduces this signal and provides some filtering before feeding into the 11th order elliptical filter.

The VCA is a current mode device and should be fed with a signal with 0 dc offset via C45 and R111. Distortion is trimmed with RV12.

The B Half of the circuitry is identical in operation to that just described.

Voltage Controlled Filter
(refer schematic CMI331-05, 06, 07, 08)

The VCF is a state variable type utilising two voltage controlled integrators per stage with feedback. Two stages are used to give a 4th order characteristic. One stage only will be described as all four stages are identical.

C51 isolates any DC component, L15 pin 1 is a high pass output. IC L15 pin 7 is a band pass output and J11 pin 1 is the low pass output.

R115 and IC J15 (VCA) operate as a variable feed in resistor to the integrator formed by IC L15 (pins 5,6 & 7) and C47. Similarly, R114, IC K15, IC J11 (pins 1,2 & 3) and C43 operate as a voltage controlled integrator.

RV7 and RV8 adjust the symmetry of each VCA for minimal distortion but have only a minor effect at low frequencies, see the diagnostic section for the correct adjustment procedure.

Each op amp stage of the VCF feeds back into a common node at pin 2 of IC L15. Varying the control voltages to the two integrators so their frequency response changes alters the output frequency response.

Mixing and VCA Buffers

(*ref schematic CMI331-09*)

The VCAs are a current mode device, therefore their outputs may be mixed before buffering. For this purpose a 4053 analog switch is used (note that its power supply is not +-V but +vref and -vref)

The current outputs from the VCAs are fed into analog switch IC M9,10 (4053) this operates in current mode to switch the signals to IC L8 (5532) or to mix them into pin 15 of IC M9,10. C57 limits the bandwidth of the mixed signal to reduce noise power and assist with the stability when mixing is switched out.

When mixing is not used the currents from the VCAs pass directly through IC M9,10 and are converted back to voltage signals by IC L8. For mixing the A and B signals the currents from the VCAs are switched into a summing node at pin 3 and 13 of IC M9,10 where the signal is converted back to voltage by R133 and again to current by R107 and R108. R134 and R135 help improve stability and reduce noise.

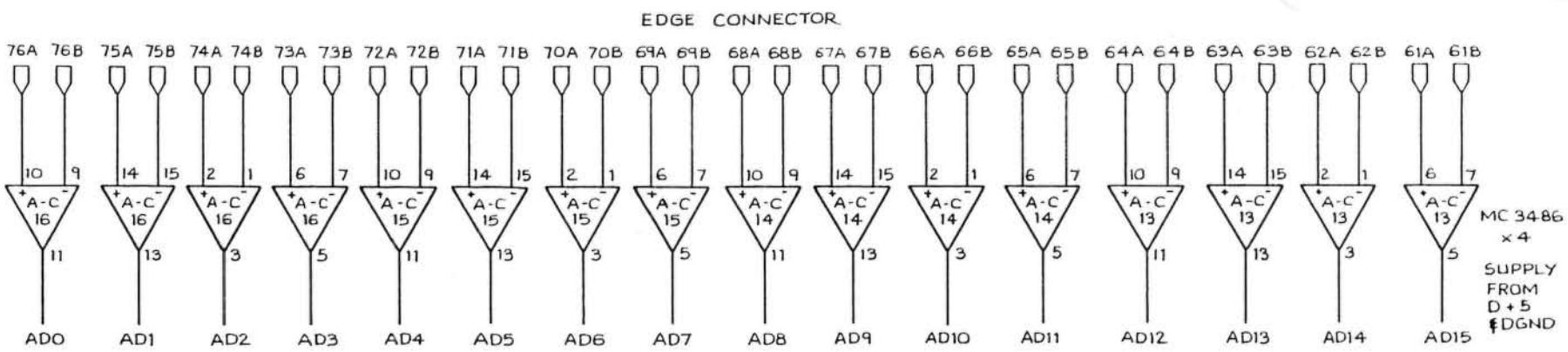
R136 ensures that mixing is off when no control is present.

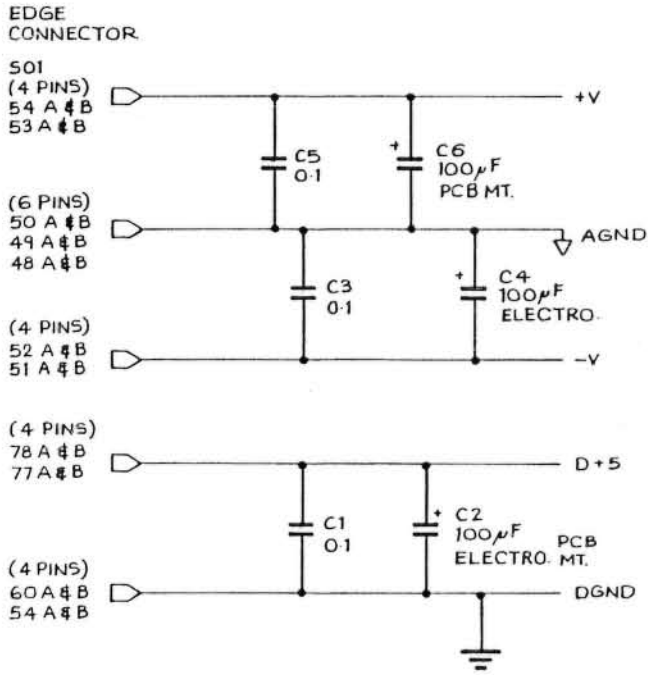
IC L8 converts the current signals to voltage and drives the output buffers.

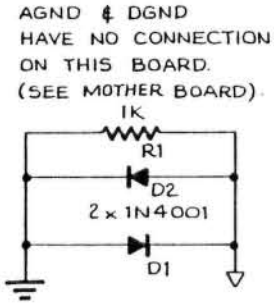
Calibration Procedure

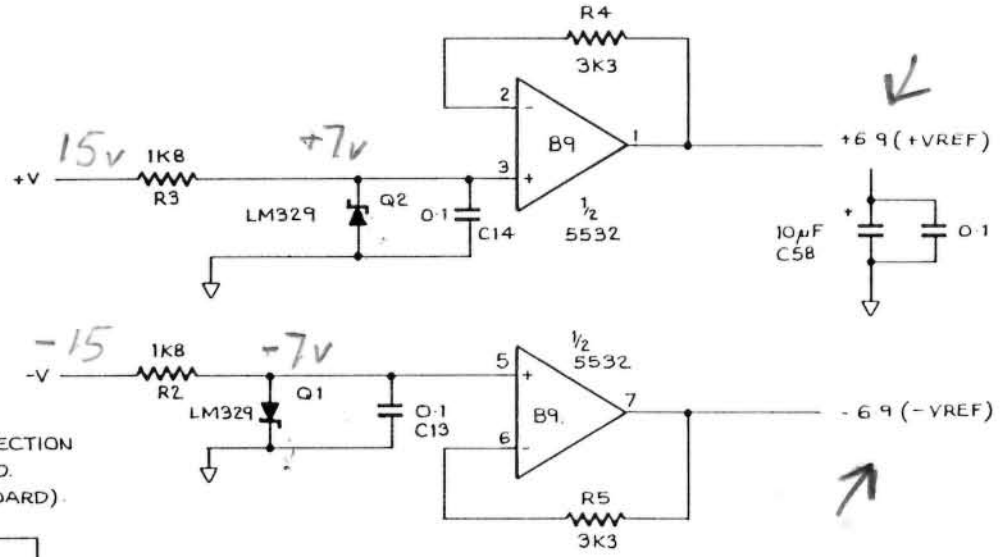
The calibration procedure is fully described in the diagnostic section of this manual.

This procedure requires a minimum of a 20MHz bandwidth CRO, an accurate noise,distortion and power meter and a digital multimeter in addition to other normal tools.







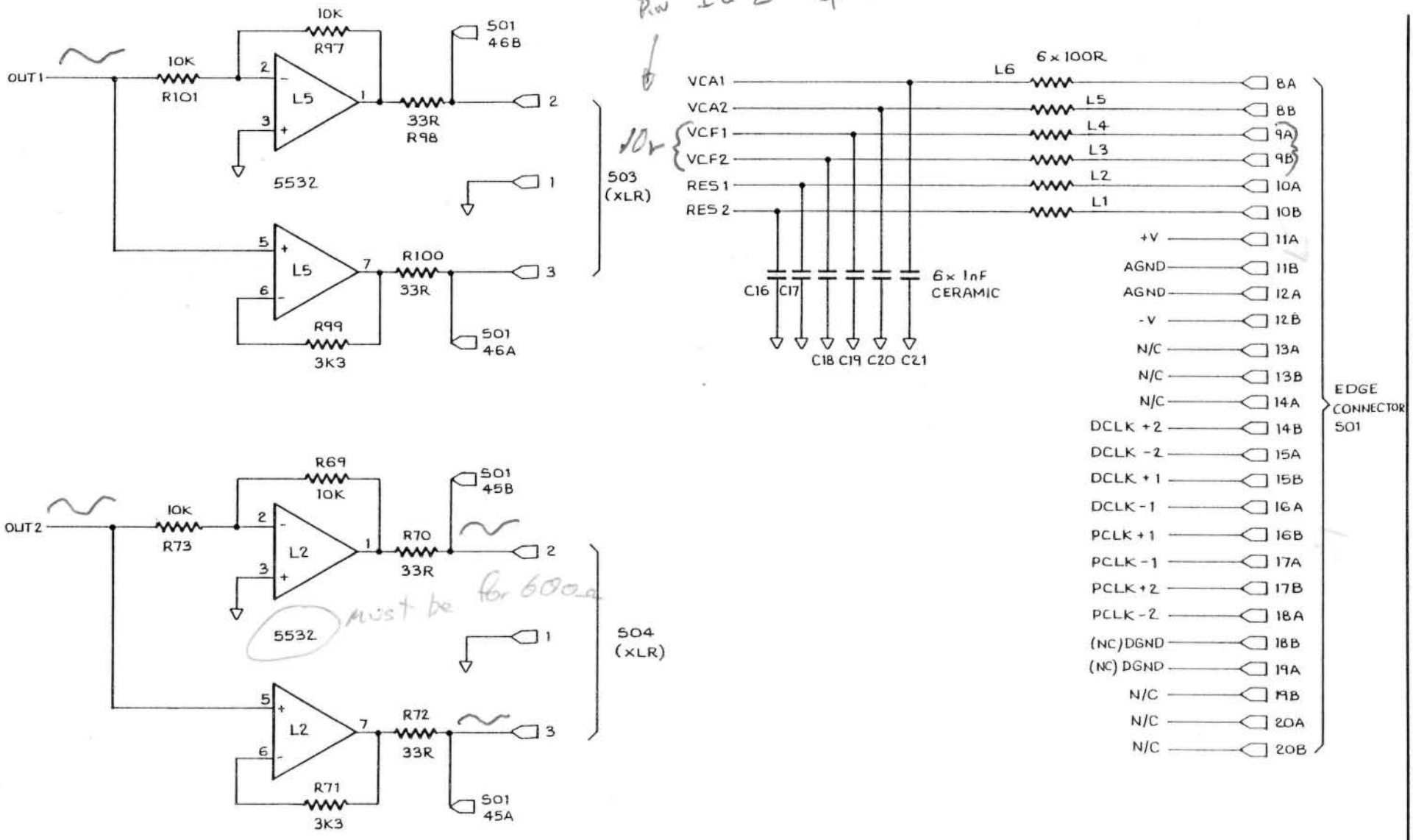


Data Buffers, Power Supplies and Voltage References

DRAWN: RH REVISION: 1B.1

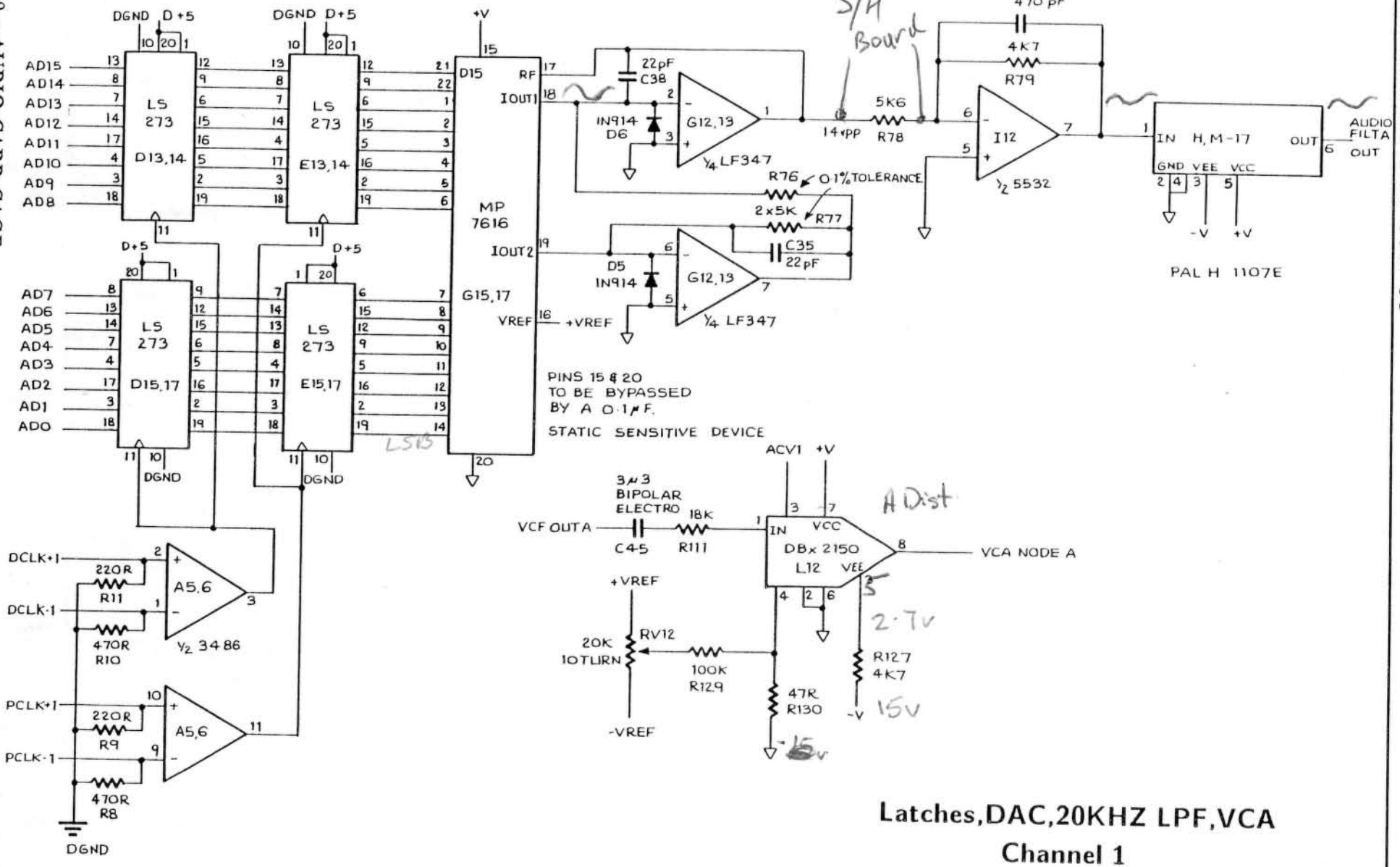
(F3) other 2 VCA

Pin 1 & 2 Top row



Output Drivers, Inputs From Channel Card

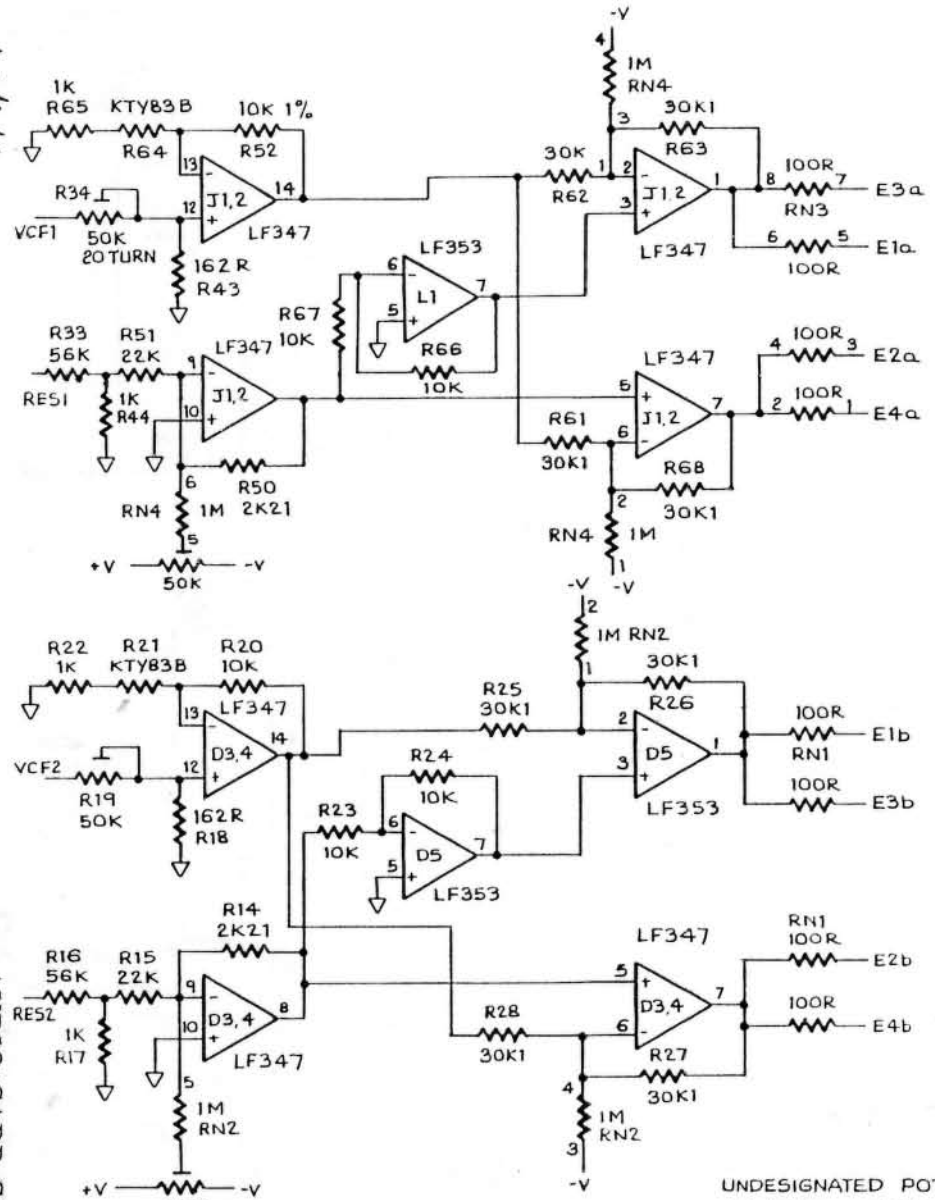
DRAWN: RH REVISION: 1B.1



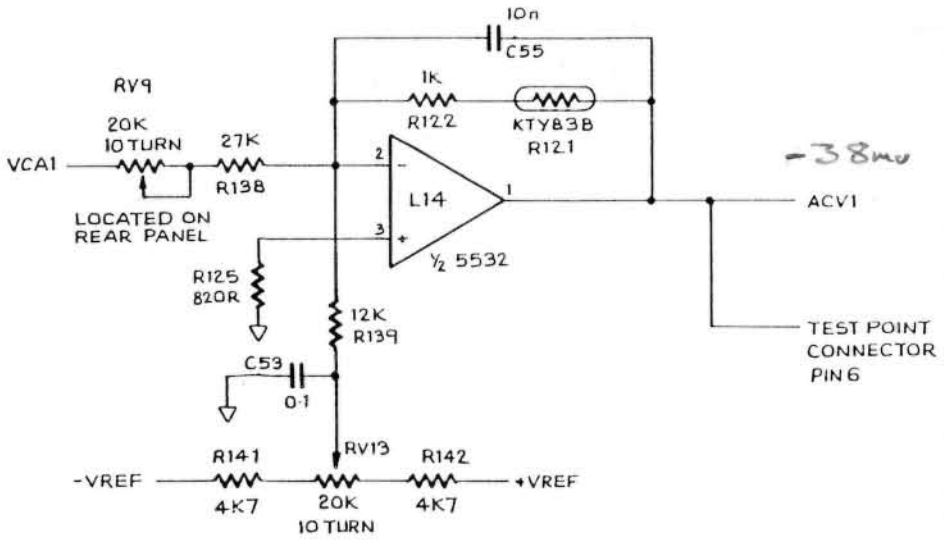
Latches,DAC,20KHZ LPF,VCA

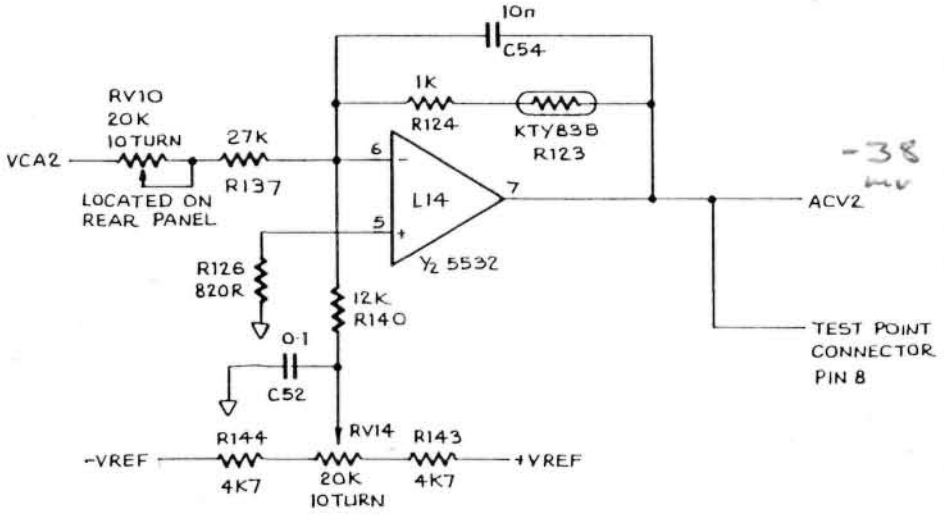
Channel 1

DRAWN: RH REVISION: 1B.1



UNDESIGNATED POTS ARE MOUNTED ON TOP OF IC S J1,J2, F1, D3, D4 & D5



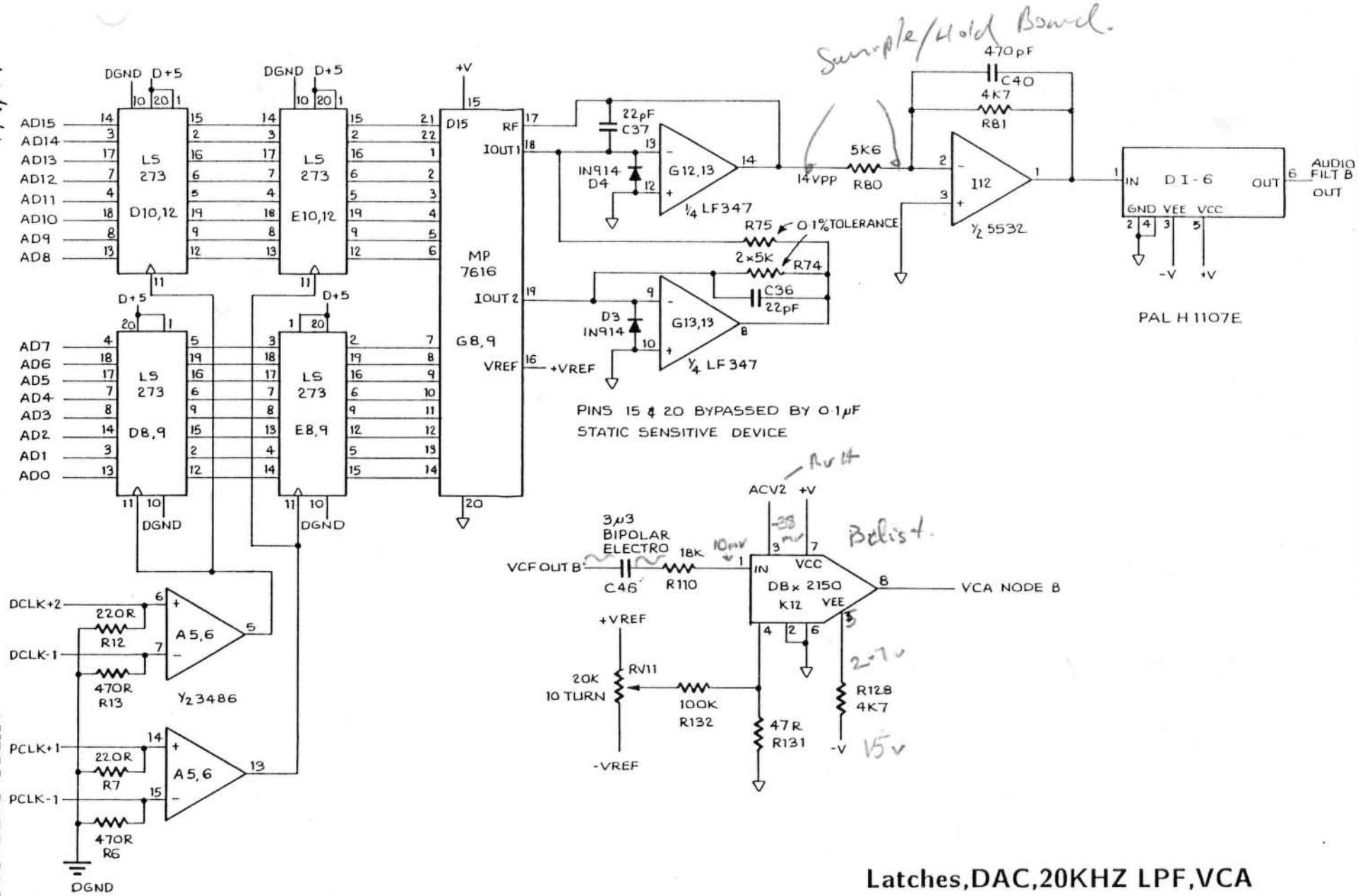


Voltage Controls For VCA'S &VCF'S

DRAWN: RH REVISION: 1B.1

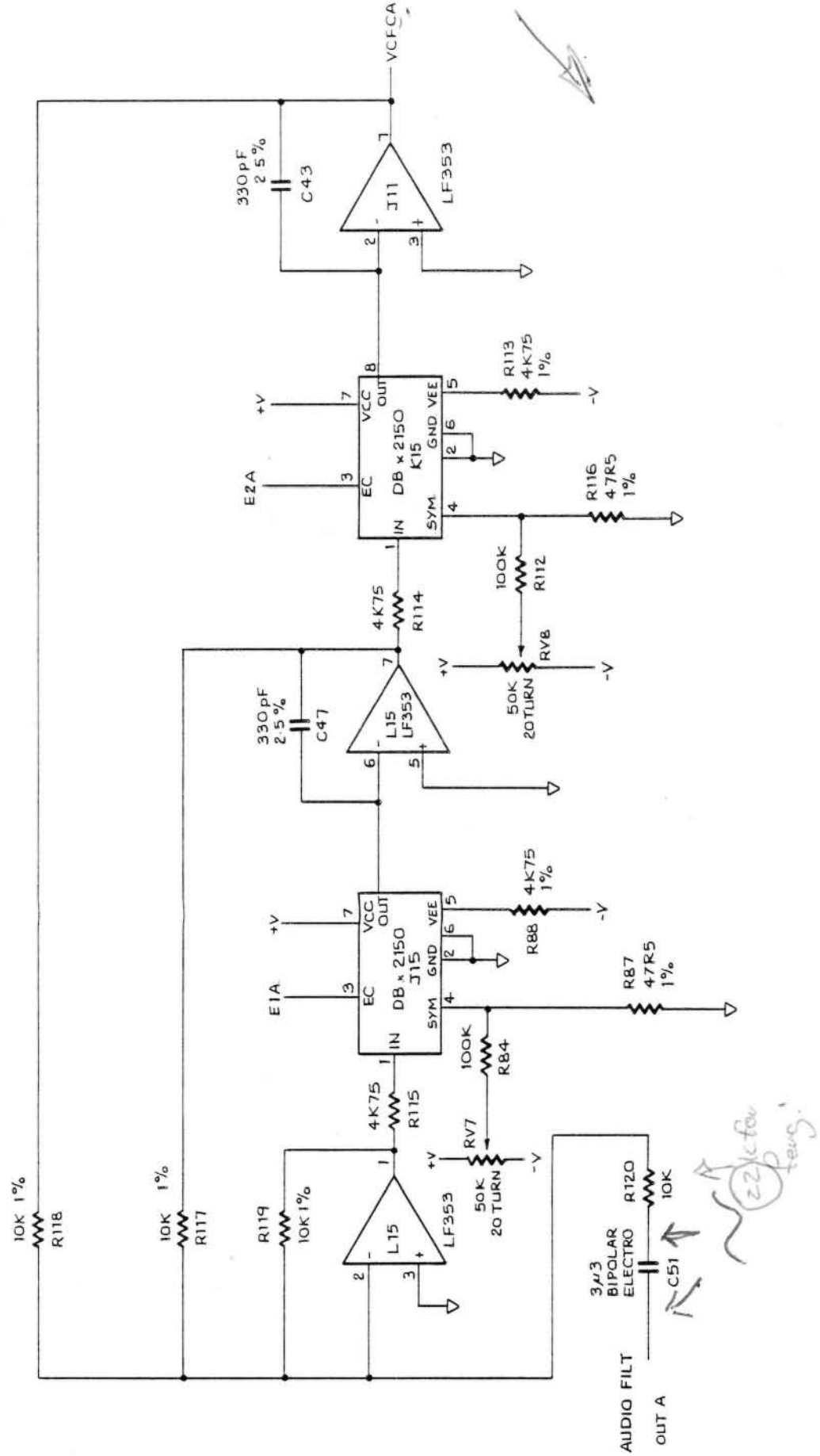
Audio Card CMI-331-02

AUDIO CARD CAGE - 3.2.9



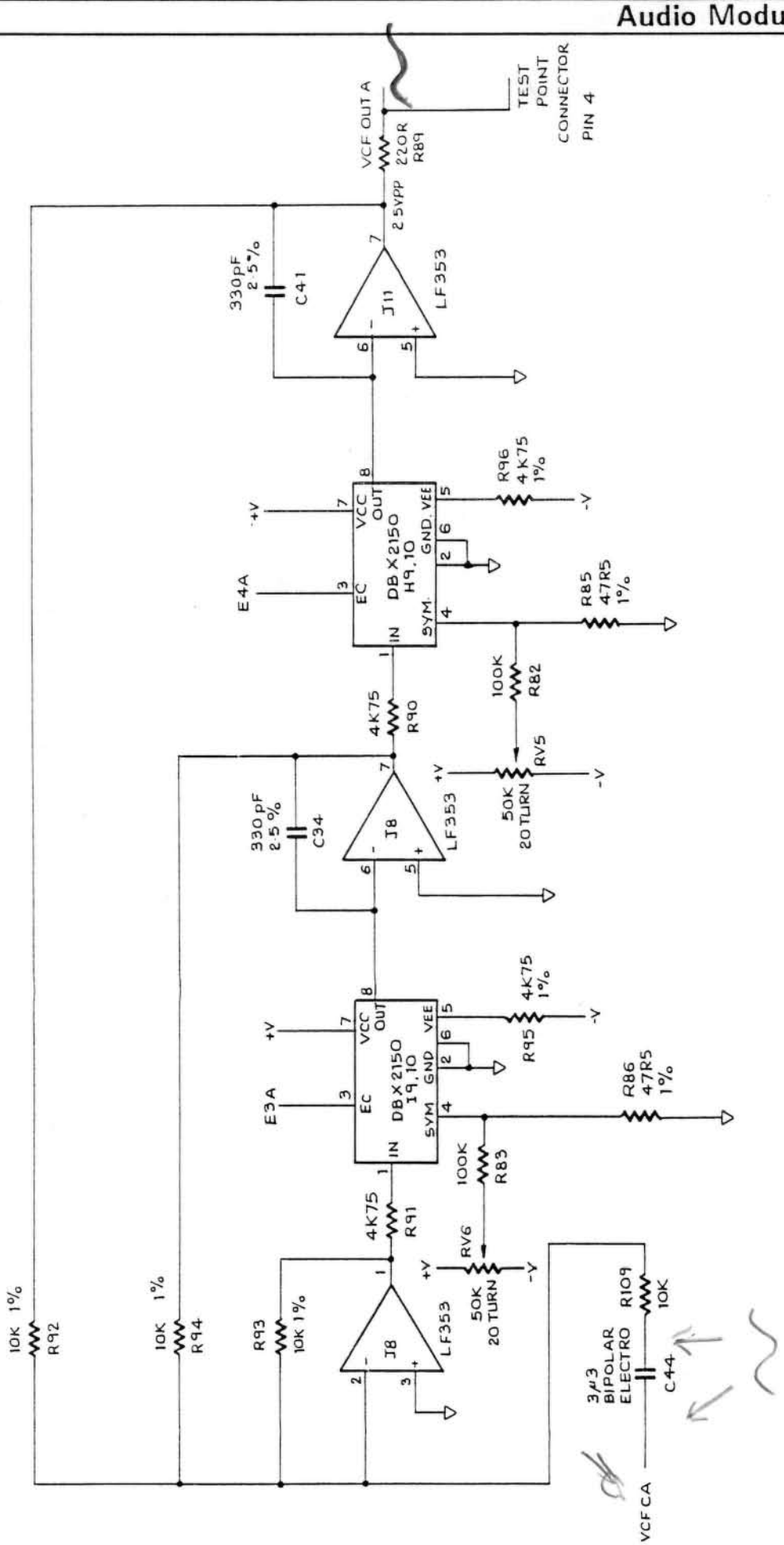
Latches,DAC,20KHZ LPF,VCA
Channel 2 (B)

DRAWN: RH REVISION: 1B.1



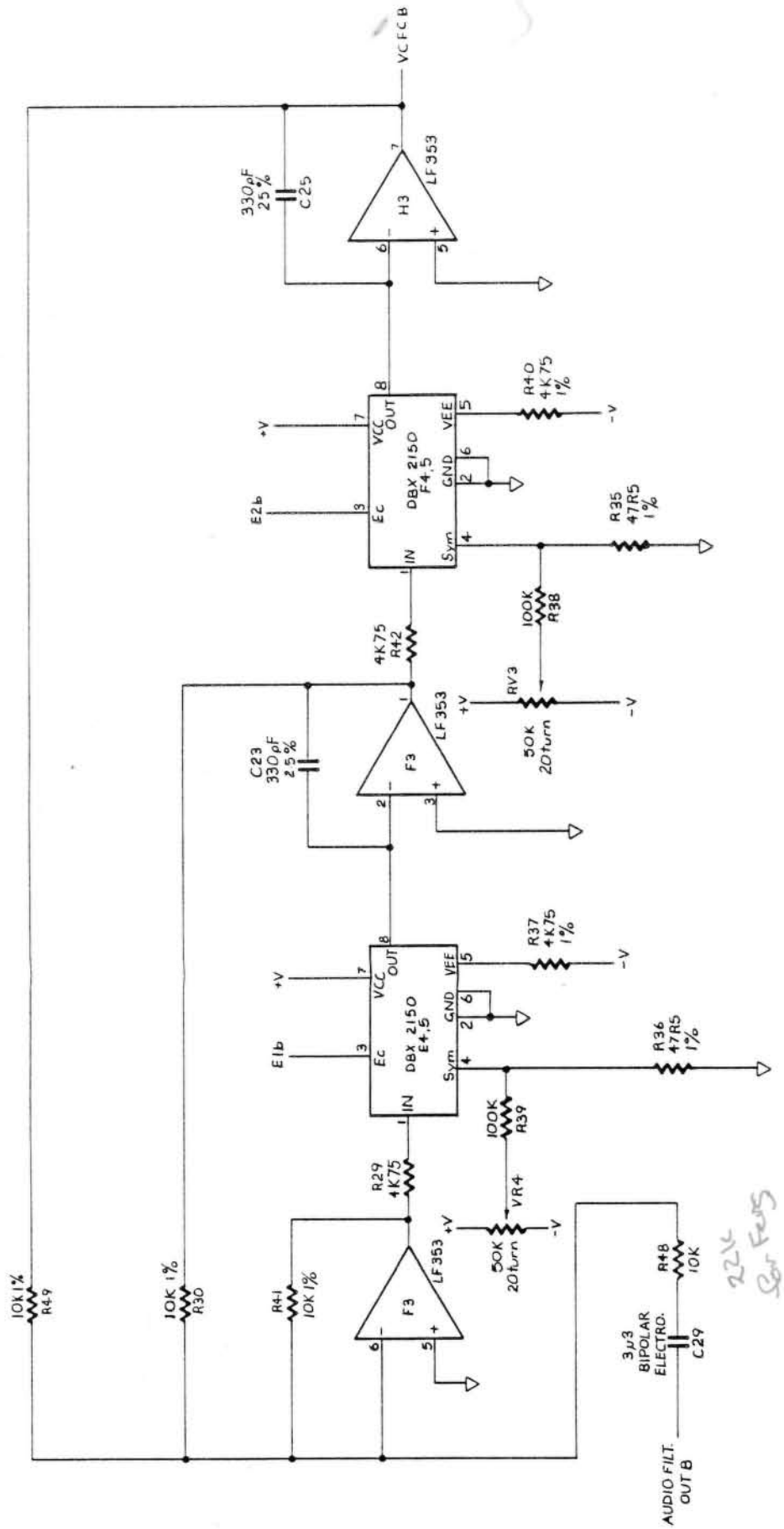
Voltage Controlled Filter Channel A Stage 1

DRAWN: RH REVISION: 1B.1



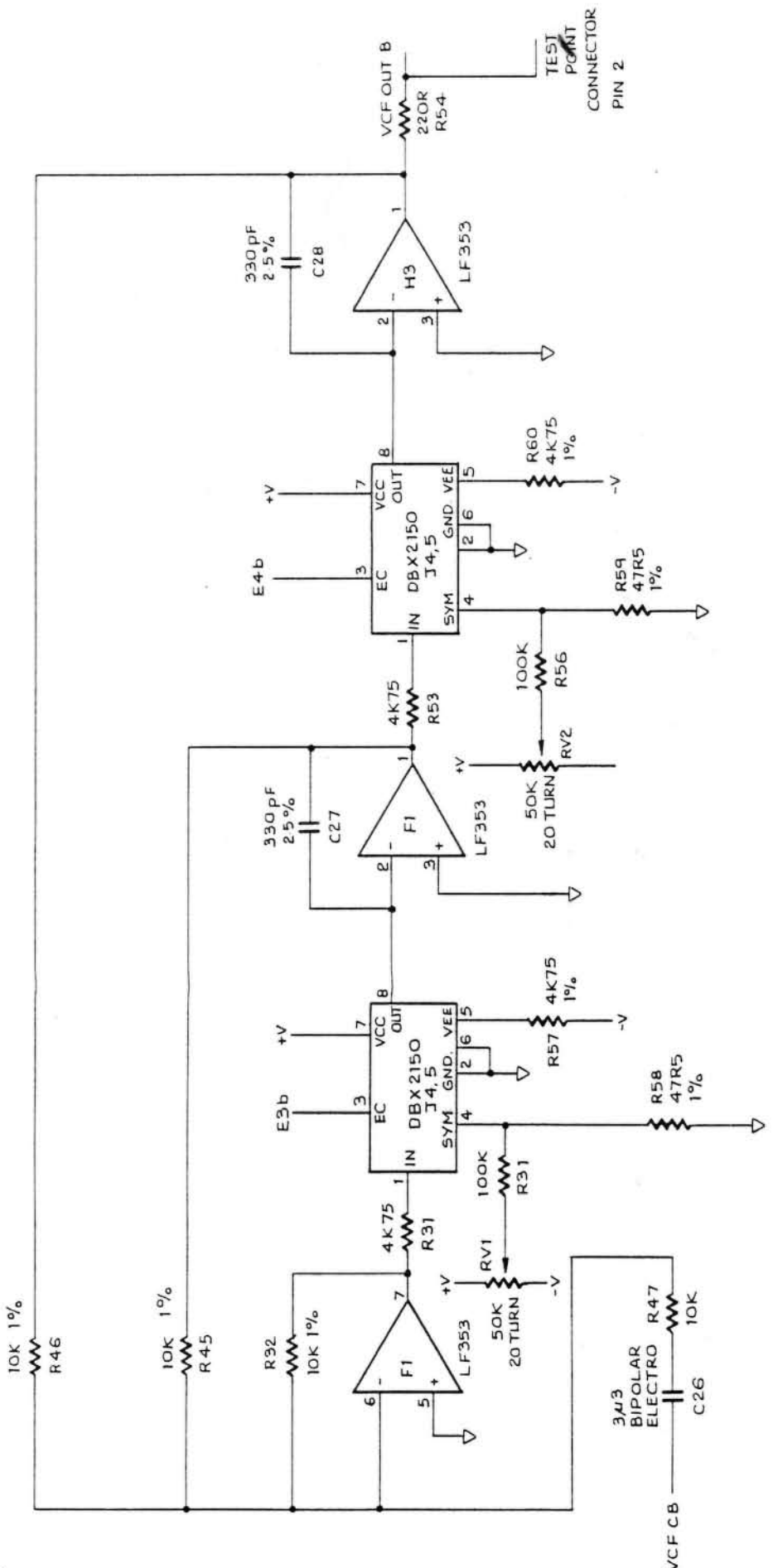
Voltage Controlled Filter
Channel A Stage 2

DRAWN: RH REVISION: 1B.1



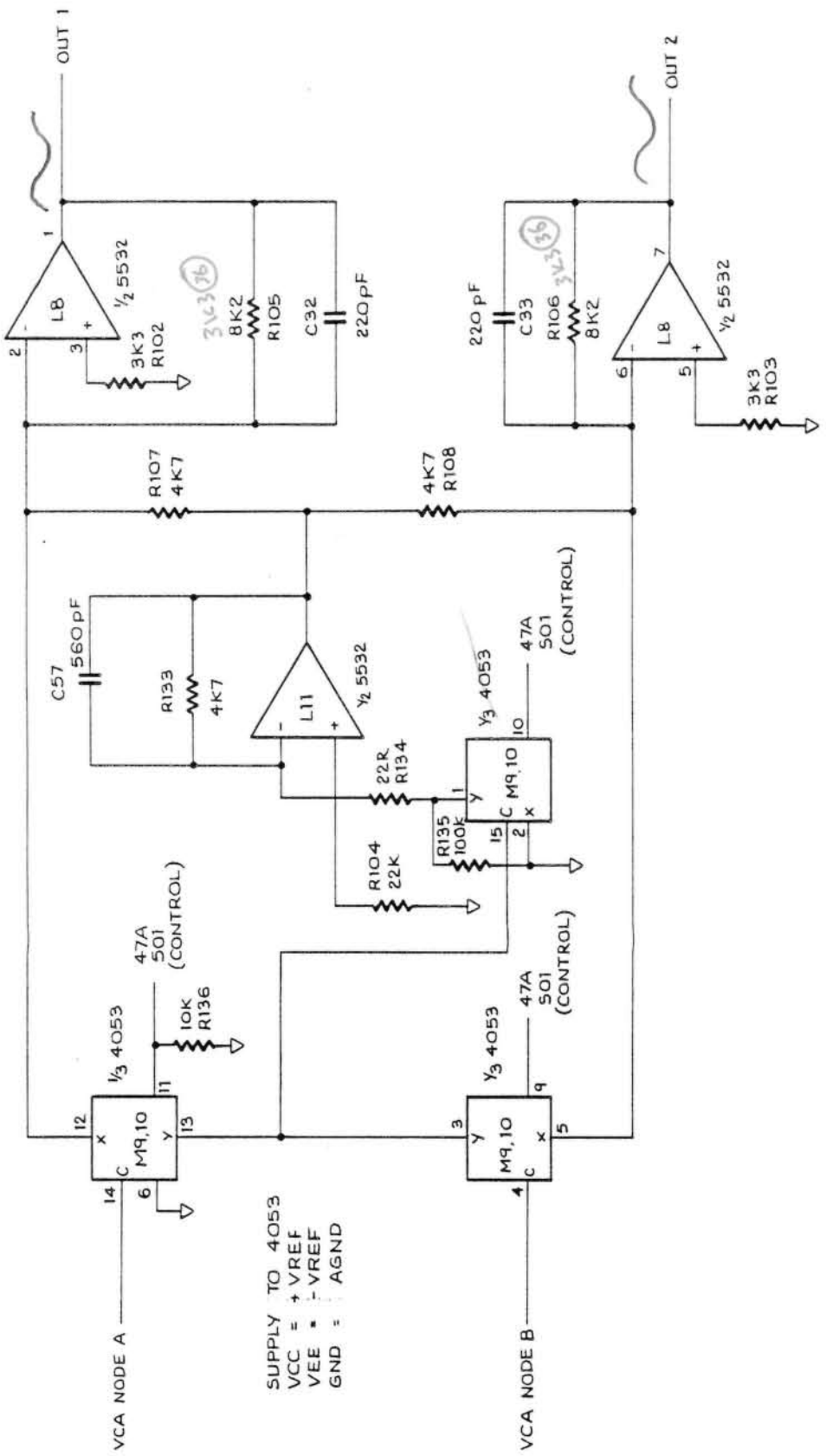
Voltage Controlled Filter
Channel B Stage 1

DRAWN: RH REVISION: 1B.1



Voltage Controlled Filter
Channel B Stage 2

DRAWN: RH REVISION: 1B.1

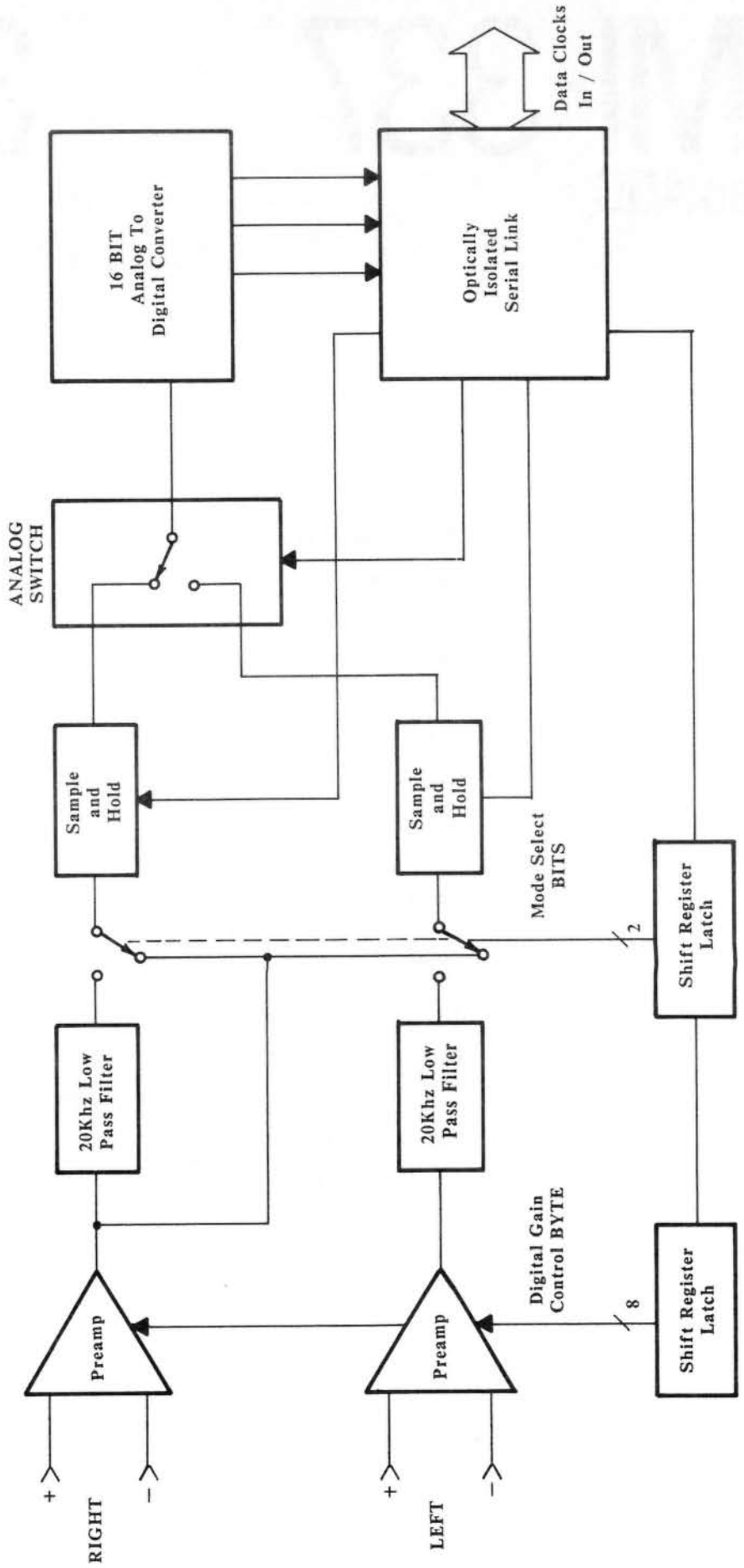


Panning Facility

DRAWN: RH REVISION: 1B.1

CMI-337 3.3
Stereo ADC

Stereo ADC Block Diagram



Terminology
WP: Waveform Processor
CC: Channel Card
ADC: Analog to Digital Converter
TH: Track and Hold
MDAC: Multiplying Digital to Analog Converter
LPF: lowpass filter

Introduction

The Stereo ADC is the means by which real sounds are digitized to 16 bits into the Series III CMI. It connects via an optically isolated serial link to the WP and is situated in the Audio rack. The sampling rate is determined by the pitch set on side A of CC 1. The ADC operates in mono, stereo and in a filter bypassed high speed mono mode. Mono and stereo allow sample rates to approximately 50k and the unfiltered mode allow rates to approximately 100k. The mode of operation and the input level is controlled by a 16 bit word in the WP address space. Data from the ADC is read from a 16 bit location in the WP address space.

Analog signal chain

The stereo balanced inputs are converted to single-sided signals in the first gain stage and then fed through MDACs, for software gain control of the sampling level. For best performance, the user should always select the maximum level which will not cause clipping. Anti-aliasing low-pass filters are fixed at 20kHz. The stereo channels are then fed through two Track and Holds running out of phase with each other. That is, when the right is in hold mode, the left is in track mode. The output of the track and hold that is in hold mode at any one time is feed to the input of the ADC via the an analog switch. The switching between track-and-holds occurs at the sampling frequency.

Mode selection

A 16 bit control word on the CMI-337 is used to control the selection of mono and stereo sampling, the input level, and the bypassing of the fixed lowpass filters. The mono/stereo mode bit is also used to synchronize the receiving of the right and left samples by the WP software when in stereo mode. This occurs before a sample actually starts being read by the WP. It is occurring continuously when the level meters on the sampling page are being processed.

Clocks and control

The ADC needs a 1.78MHz clock to operate. The other timing signals come into and out of the CMI-337 via the optically isolated interface. This interface consists of current drivers on output signals and opto isolators on input signals. The ADC chip itself generates the clock signals to load the 16 bit data into and out of the WP. These clocks occur in 16-pulse bursts when the ADC is given a start conversion command. The start conversion command is generated from the rising edges of the clock originating from Channel Card 1, side A which is transmitted to the CMI-337 through the optical link from the Waveform Processor.

Input preamps and low pass filters

(ref schematic CMI-337-01)

Low noise NE5534 amplifiers are used to receive the balanced inputs and make them single ended. These input amplifiers have a gain of 3.8 and 18 volt supply rails to allow them to handle inputs with levels ranging from +4dbm to -10dbm.

The input stages then drive the reference inputs of AD7524 MDACs via large capacitors to remove and DC offset. The MDACs allow software control of input signal attenuation by multiplying the input signal by the number from the WP. The Digital attenuation value comes from the most significant 8 bits of the CMI-337's control word at A7 via isolating RC networks.

The output of the right channel MDAC goes to both a fixed low pass filter and a resistive attenuator. One of the two outputs are selected by a relay whose function is to allow the fixed filter to be bypassed in high speed mono sampling mode.

The output of the left channel MDAC goes only to a fixed lowpass filter.

The fixed 11th order lowpass filters have a corner frequency of 20khz and passband gain of one half. To get the best noise and distortion performance, the input levels should be about 3 volts peak to peak.

In high speed mono sampling, the output of the right channel's MDAC is fed into both channels of track-and-hold and the fixed low pass filter is bypassed.

The last stage in each channel is an amplifier with a gain of 4.7 to bring the level up to that needed by the ADC of 10 volts peak to peak. This stage also has a DC servo feeding from the outputs of the track and holds to null DC offsets in each channel. The DC servo is basically an inverting integrator with a long time constant that generates a DC offset error voltage that is fed back into the gain stage. The cancelling of DC between the two channels is important in the high speed mono sampling mode. In this mode, alternate samples come from alternate track-and-holds, so that any DC offset between the two will result in severe distortion as every second sample would be displaced from its correct level by the offset.

Track and Holds

(refer schematic CMI-337-02)

The track-and-holds are constructed around high current drive voltage followers, an analog switch, a polystyrene capacitor and a JFET input opamp buffer. When the switch is closed, the voltage on the 2n2 capacitor follows the input signal. When the switch is open the voltage on the capacitor is held.

The hold control inputs are clocked on opposite phases of the clock from the WP, divided by two by D10 so that when the right track-and-hold is holding, the left TH is tracking.

Channel Multiplexing and the Analog to Digital Converter
(refer schematic CMI-337-03)

The same signal that switches the track-and-holds also switches the analog switch at F8. The track-and-holds are continuously multiplexed into the JFET buffer at H10. The Track and Hold that is currently in Hold mode is always multiplexed to the input of the ADC.

Even in Mono mode, when only the right channel input is converted, the multiplexing still takes place.

The ADC is the Matsushita MA6206. On receipt of a start pulse, the ADC does a succesive approximation conversion on its input signal. This results in 16 clock pulses and data bits being generated and shifted out of the CMI-337 to the WP.

The power supply for the CMI-337 is completely isolated from the rest of the CMI with only a ground tie resistor between the two . On card regulators couple the three DC supplies to the on board components.

Control
(refer schematic CMI-337-04)

The same clock used to clock the ADC data into the WP is used to shift data from the WP into the control latch on the CMI-337. The ADC clock output consists of 15 normal pulses followed by one truncated pulse of only 100nS, for each conversion cycle. This last pulse is too short to send over the opto-isolated link so the ADC clock out is used to fire a monostable, half of C11, whose output is cabled to the WP as the data clock.

This clocking occurs each time a conversion is done. The data from the WP is latched into output latches in the 74LS595s by the end of conversion signal generated by the ADC, (the same occurs at the WP with received ADC data).

The most significant 8 bits of the control latch are used to control the Audio level. The next two bits are used to select filter bypass/mono mode and mono/stereo mode.

The conversion rate clock and the serial data from the WP are received at B10 by a high speed optoisolator. The data goes into the data input of the 16 bit control register, at A7 and B9.

The Start Conversion clock goes into a divide-by-two stage at D10 and a multiplexer formed from 3 gates of the NAND package at D11. The multiplexer is used to send either the direct conversion clock or the divided by two conversion clock to the ADC start pulse generator, formed around E11 and F11. This generates a start conversion pulse on every rising edge presented to it.

The half of D10 that feeds pin 5 of D11 is used to synchronize mode changing with conversions.

In mono mode, the divided by two signal is selected to make the ADC do a conversion only when the right channel input is present at the ADC input.

In stereo mode the direct clock is used, so that the right and left channel inputs are converted in turn.

In high speed mono, both clocks are used as in stereo but the right input is connected to both track-and-holds.

Remember that the conversion clock is a square wave that drives the track-and-holds in anti phase, and selects the Sample and Hold that is currently in hold mode to the ADC. The ADC always has a signal at its input that is being held by one of the Sample and Holds.

Before the selected conversion clock is fed to the start circuit, it is fed into a delay to allow the analog circuits to settle before starting the conversion. This is most significant on low level signals, as it is the most significant bit that will be corrupted on conversion. The result being something resembling cross over distortion. The effect is most significant on small amplitude signals, as the overshoot generated when the analog multiplexer swithces is small, but of greater amplitude than the signal being converted.

The master oscillator is made around inverters G11 and the 3.57MHz crystal. This is divided by two to clock the MA6206 and the start pulse generator.

The TTL control signals from the MA6206 are converted to currents via the diode and resistor networks coupling them to the edge connector and socket.

Control Word Bit Definitions

The control word has the following bit definitions

Bit	Function
15	most significant bit of preamp attenuation
14	
13	
12	
11	
10	
9	
8	least significant bit of preamp attenuation
7	bypass Low Pass Filters
6	sample mode control
5	n/c
4	n/c
3	n/c
2	n/c
1	n/c
0	n/c

Bit 7 Bypass Low pass filters

This bit does 2 things. It bypasses the 20 KHz LPF and connects the output of the right channel preamp into both sample and holds, to allow mono sampling at greater than 50 KHz. Sampling at greater than 50KHz in mono can be done without switching this bit, but at the expense of reduced capture time for the track-and-hold and hence increased distortion.

Bit 6 Sample Control

This bit selects whether the ADC does every sample or every second sample.

Every Sample is used for mono at greater than 50KHz with the filters switched out or stereo.

Every second sample is used for mono sampling at less than 50KHz.

With the Channel card pitch set at P, then the sampling frequencies and modes will be:-

Bit 7	Bit 6	Result
0	0	Stereo sampling at P/2 per channel.
0	1	Mono sampling at less than 50KHz at P/2 .
1	0	Mono sampling at greater than 50KHz at P.
1	1	Mono sampling at greater than 50KHz at P/2. (Invalid)

CALIBRATING THE CMI-337 ADC CARD (Rev 3)

CH1 means channel 1 of the CRO
CH2 means channel 2 of the CRO
all triggering is done on channel 1.

Connect the card to either a waveform processor or test card. This will generate the square wave that is used to start conversions.

Before data can be read from the ADC, 2 trim pots on the 74LS123 at C11 must be set.

1. Start-Conversion Pulse Delay

Put CH1 on C11 pin 10. Put CH2 on C11 pin 5 and adjust RV2 so that there is a high going pulse approximately 1.5 microsecond long. This will now allow the ADC to receive convert commands via F11 pin 9.

2. Data Clock Pulse Length

To allow data to be transmitted from the ADC card, Trimpot RV1 must be calibrated.

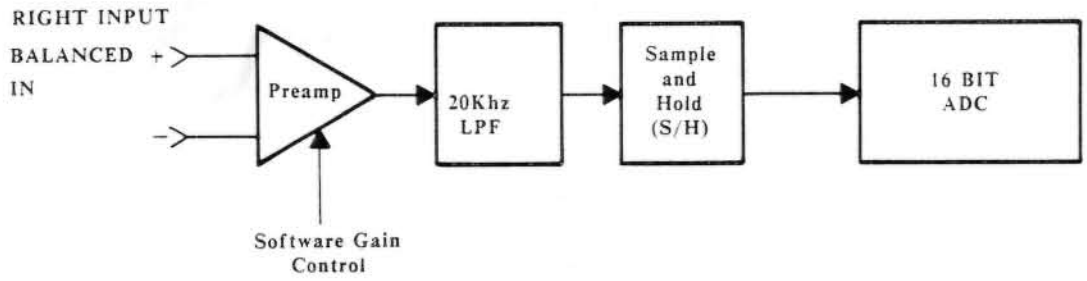
Put CH1 on F11 pin 9. Put CH2 on C11 pin 4. Adjust RV1 so that the pulses on CH2 are 50% duty cycle.

This adjustment is needed to stretch the last pulse from the ADC to allow it to be sent down the current loop.

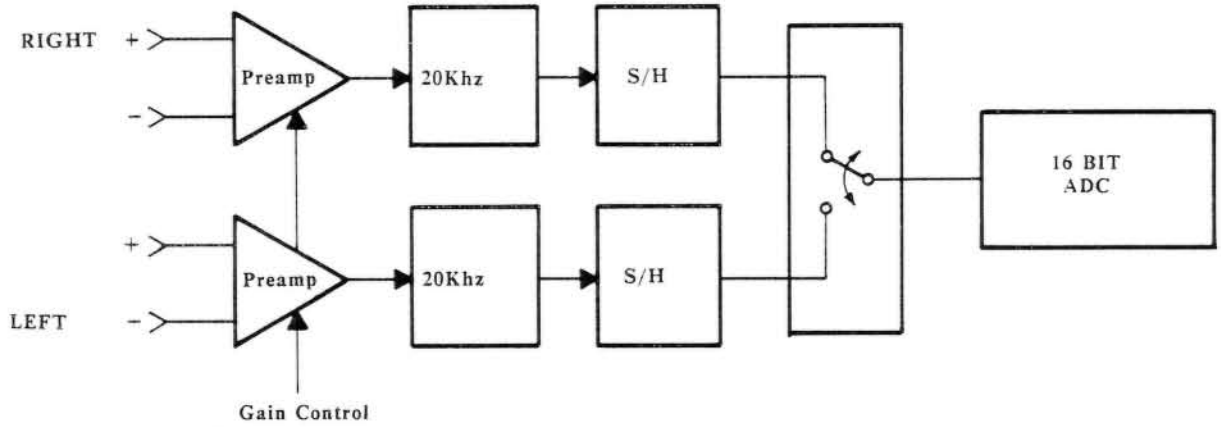
At this point the CMI-337 should be able to run with the CMI software. Messages such as "Sample fault" mean that the above adjustments haven't been made, that there is no power to the CMI-337 or that the CMI-337 is not plugged in correctly.

The 3 Modes of Operation of The ADC

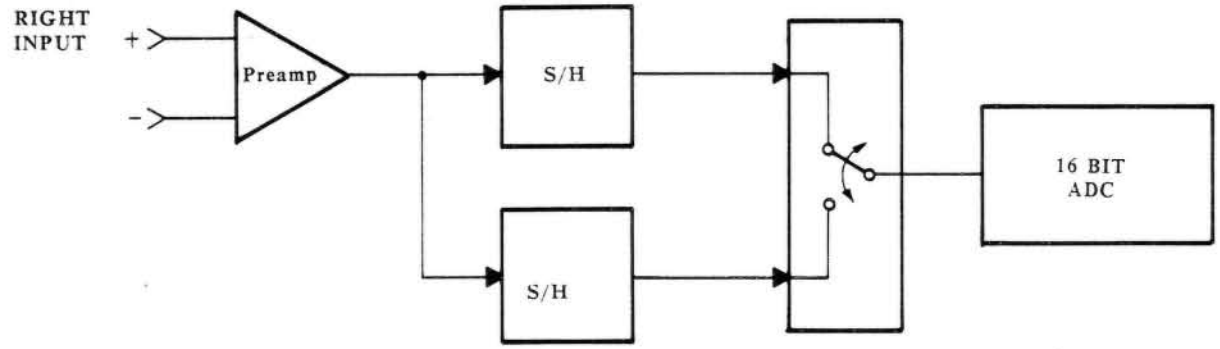
MONO MODE (50Khz or Less)

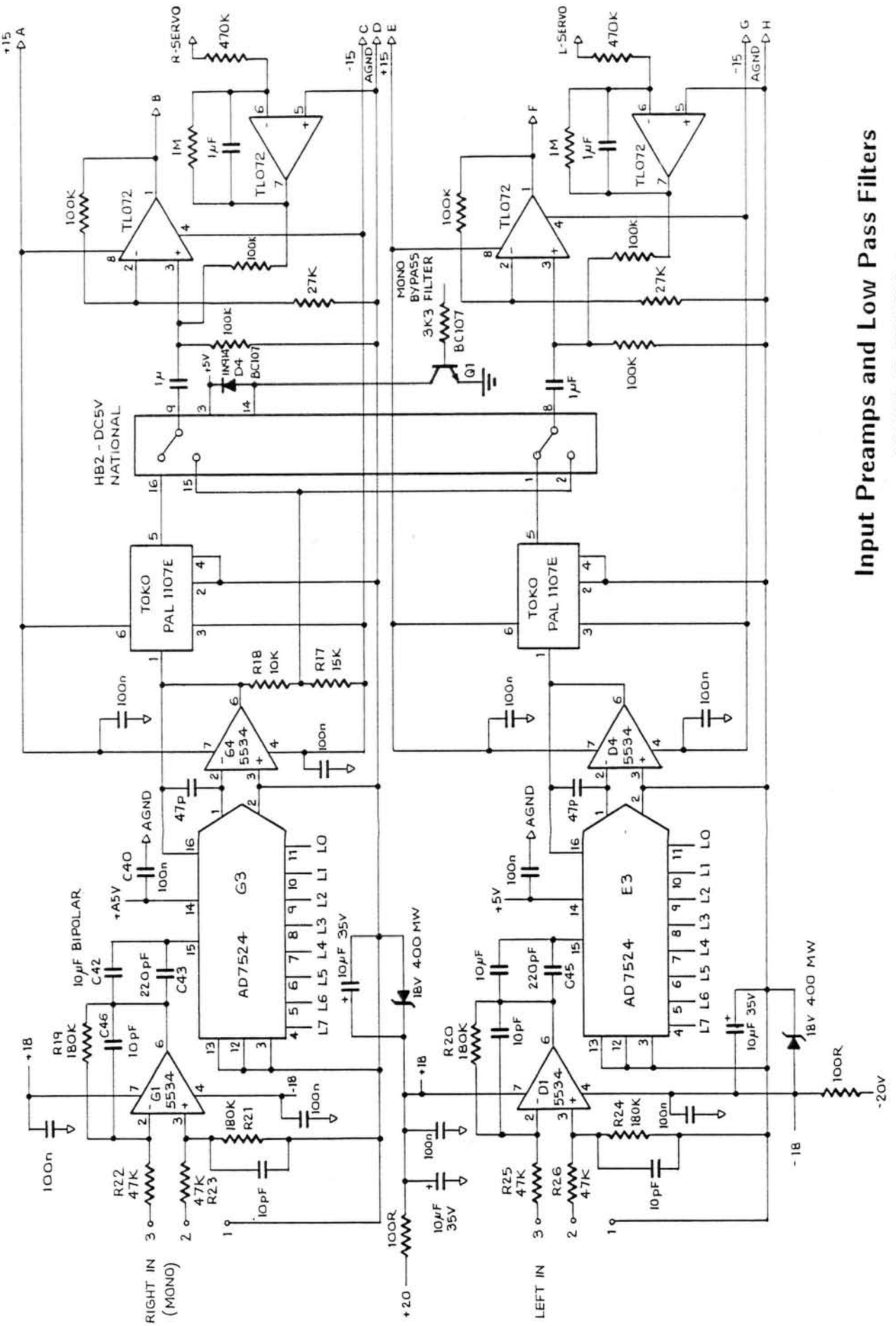


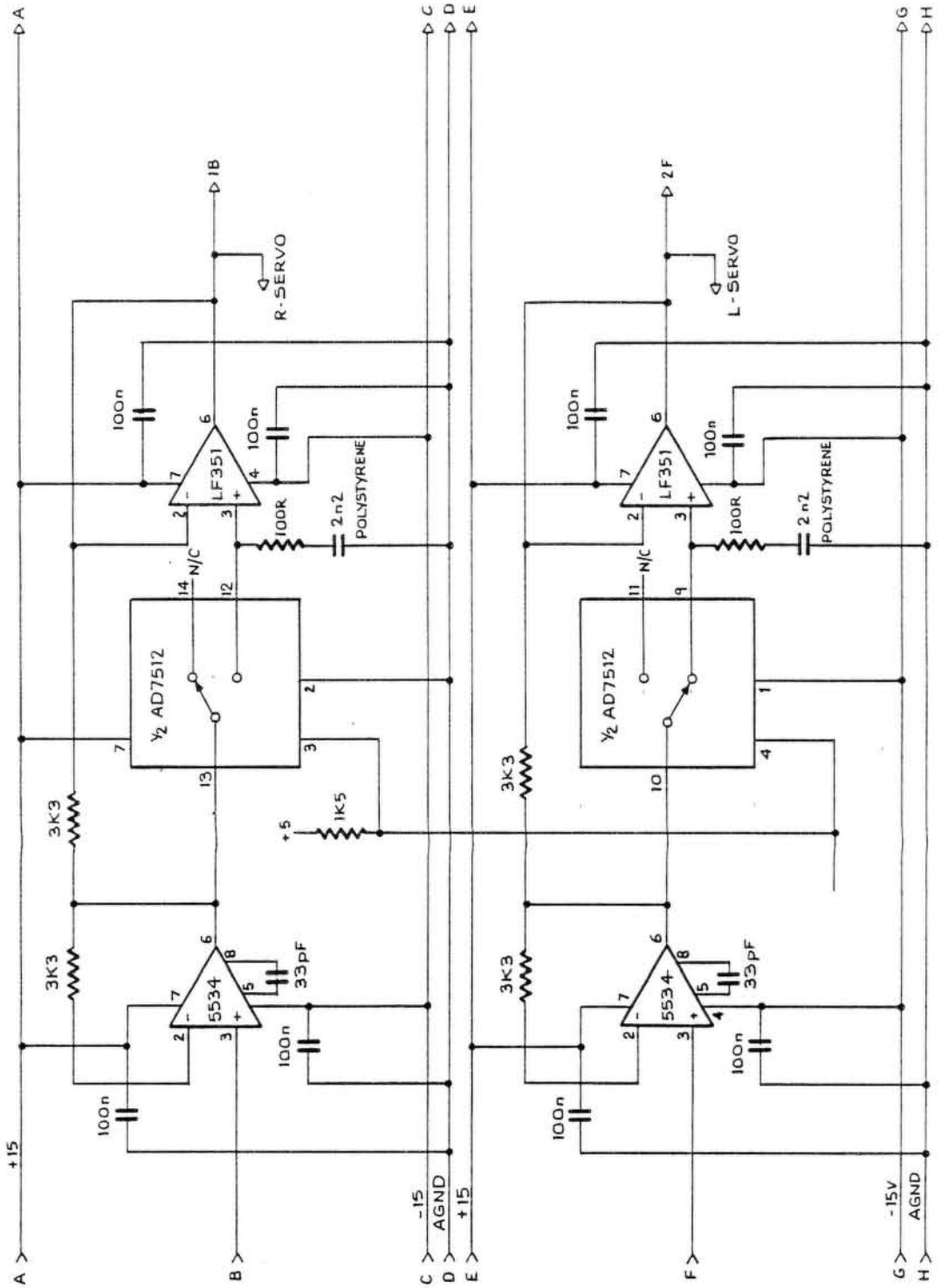
STEREO MODE (UP TO 50Khz A Channel)



MONO MODE (Greater Than 50Khz)

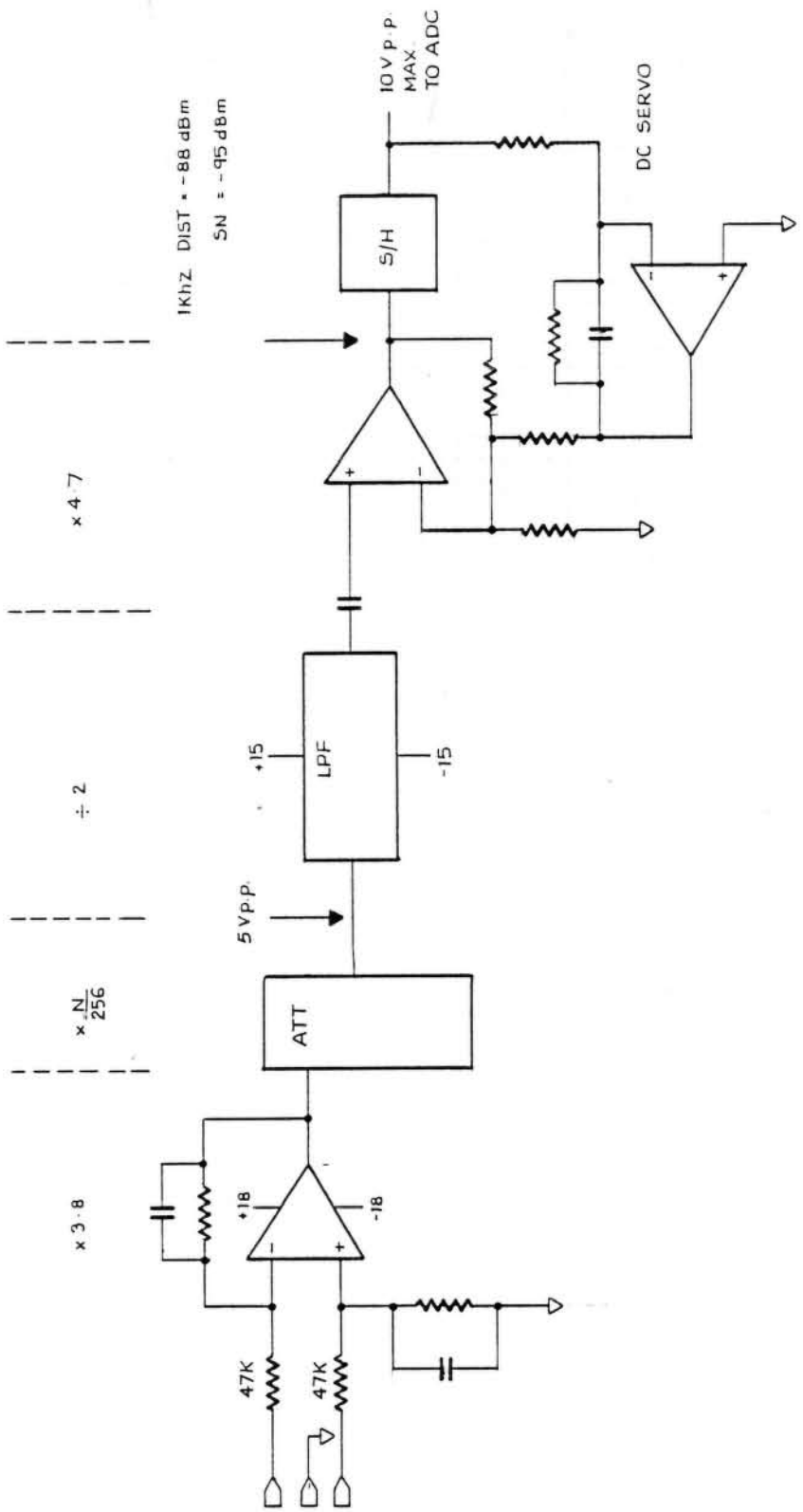



Input Preamps and Low Pass Filters
DRAWN: AB REVISION: 3
R-SERVO
L-SERVO
470K
TL072
100K
1M
1µF
27K
MONO BYPASS FILTER
3K3
BC107
IN914
D4
Q1
HB2 - DC5V NATIONAL
TOKO PAL 1107E
R18 10K
R17 15K
100n
47P
AGND
+A5V
+5V
+18
-18
-20V
C40
C42
C43
C45
C46
10µF BIPOLAR
220pF
10pF
10µF 35V
18V 400 MW
100R
AD7524
G3
E3
G1
D1
D4
5534
R19 180K
R20 180K
R21
R22 47K
R23 47K
R24 180K
R25 47K
R26 47K
RIGHT IN (MONO)
LEFT IN
+20
+15
-15
AGND



Track-and-Holds

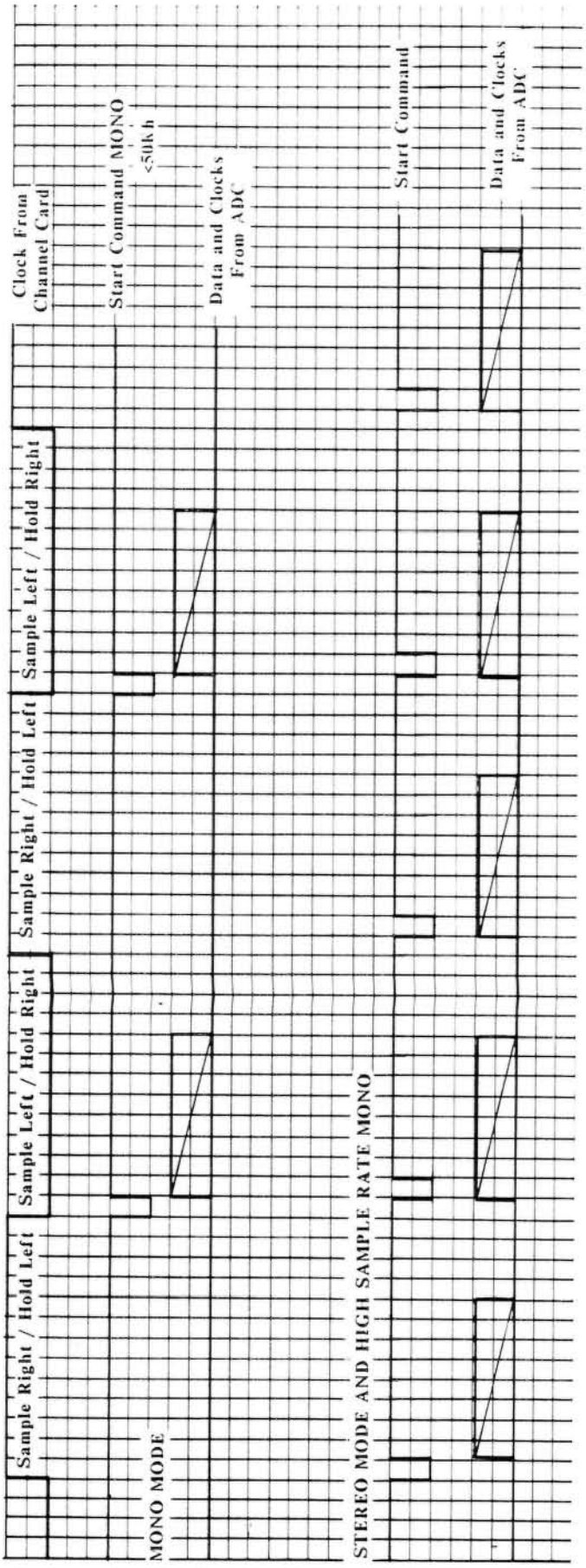
DRAWN: AB REVISION: 3



Sampling Card Gain Structure

DRAWN: AB REVISION: 3

3 Modes of Operation of ADC Timing

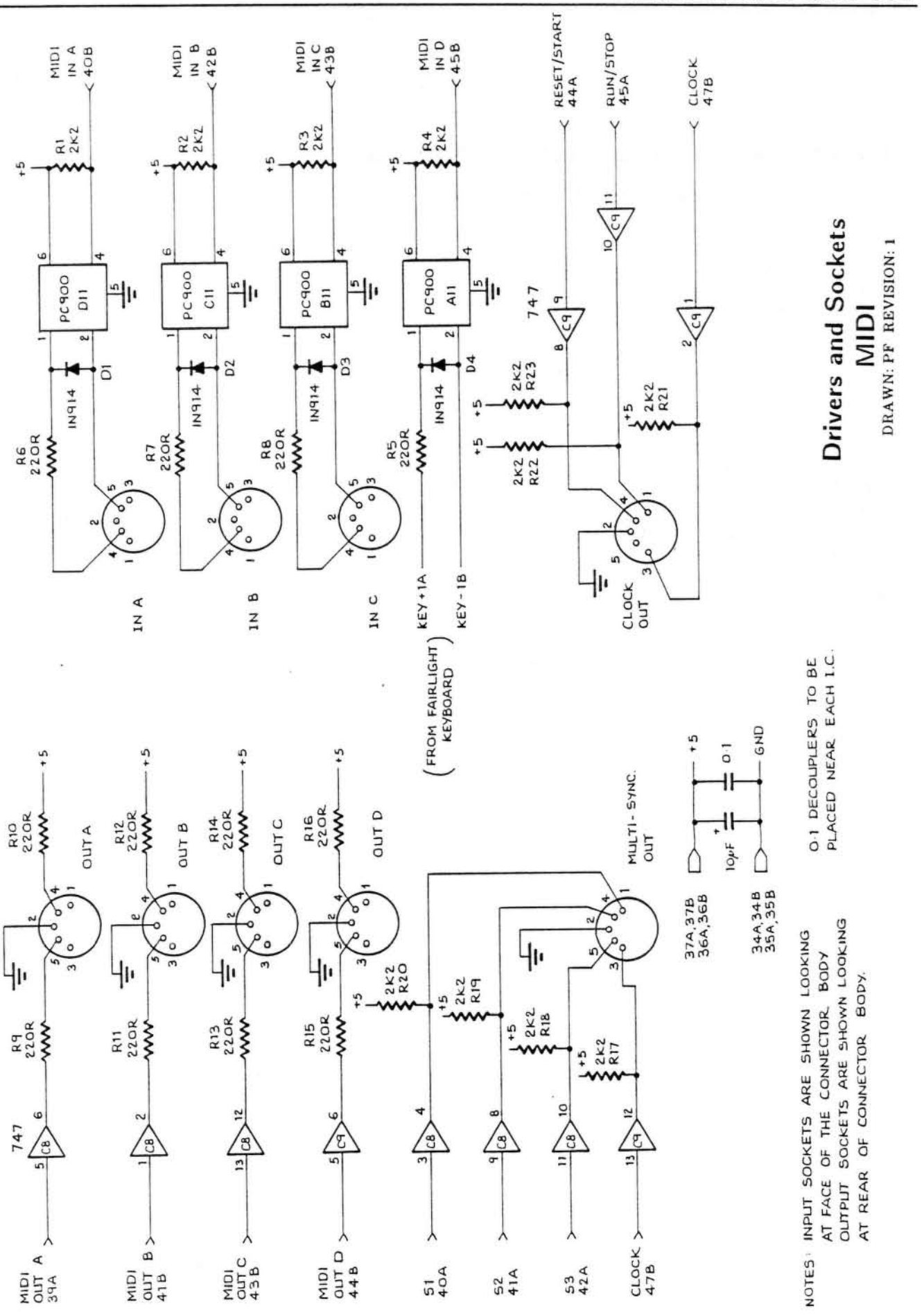


CMI-332 MIDI Module 3.4

CMI-332 MIDI Support Card

This circuit board contains the analog circuitry required for the I/O for MIDI. There are 3 MIDI inputs (A, B & C) and 4 MIDI outputs (A, B, C & D) all through DIN sockets. There is provision for a fourth MIDI input (D), this connects to the 9-way cable to the Fairlight keyboard. The MIDI I/O circuitry is the standard current loop drivers (open-collector buffers 7407 (C8,C9) and receivers (fast opto-couplers PC900 (A11,B11,C11,D11)).

There are two other output (5-pin DIN) sockets. One is the CLOCK output, containing the CLOCK, RESET/START and RUN/STOP TTL compatible signals. This CLOCK output is designed to control Roland drum machines, etc. The other is the multiple SYNC output. A click or sync signal received through the CLICK input is fed to the 68B40 Timers (see above). The outputs are connected to the DIN socket driven by open-collector buffers. You will notice that the SYNC out 4 signal is the same as that of the CLOCK and of CLICK out.


MIDI IN A 40B
MIDI IN B 42B
MIDI IN C 43B
MIDI IN D 45B
RESET/START 44A
RUN/STOP 45A
CLOCK 47B
R1 2K2
R2 2K2
R3 2K2
R4 2K2
PC900 D11
PC900 C11
PC900 B11
PC900 A11
IN914
D1
D2
D3
D4
R6 220R
R7 220R
R8 220R
R5 220R
IN A
IN B
IN C
KEY+1A
KEY-1B
(FROM FAIRLIGHT KEYBOARD)
2K2 R23
2K2 R22
2K2 R21
747
C9
CLOCK OUT
R10 220R
R12 220R
R14 220R
R16 220R
OUT A
OUT B
OUT C
OUT D
R9 220R
R11 220R
R13 220R
R15 220R
2K2 R20
2K2 R19
2K2 R18
2K2 R17
C8
MULTI-SYNC. OUT
37A,37B
36A,36B
34A,34B
35A,35B
+5
0.1
10µF
GND
MIDI OUT A 39A
MIDI OUT B 41B
MIDI OUT C 43B
MIDI OUT D 44B
51 40A
52 41A
53 42A
CLOCK 47B
Drivers and Sockets
MIDI
DRAWN: PF REVISION: 1
NOTES: INPUT SOCKETS ARE SHOWN LOOKING AT FACE OF THE CONNECTOR BODY
OUTPUT SOCKETS ARE SHOWN LOOKING AT REAR OF CONNECTOR BODY.
0.1 DECOUPLERS TO BE PLACED NEAR EACH I.C.

Pin Connections for the 26-way Connector

(between the CMI-28 and CMI-332 and CMI-333)

Pin 1 MIDI out A.
Pin 2 +5 volts.
Pin 3 MIDI in A.
Pin 4 SYNC out 1.
Pin 5 MIDI out B.
Pin 6 SYNC out 2.
Pin 7 MIDI in B.
Pin 8 SYNC out 3.
Pin 9 MIDI out C.
Pin 10 Digital Ground.
Pin 11 MIDI in C.
Pin 12 Digital Ground.
Pin 13 MIDI out D.
Pin 14 RESET/START.
Pin 15 MIDI in D.
Pin 16 RUN/STOP.
Pin 17 SMPTE code in.
Pin 18 Digital Ground.
Pin 19 SMPTE code out.
Pin 20 CLICK out; SYNC out 4.
Pin 21 CLICK in.
Pin 22 (CMI332-3) Analog Ground.# (CMI28) n/c.*
Pin 23 (CMI332-3) +15 volts.# (CMI28) CPU Halt switch.*
Pin 24 (CMI332-3) -15 volts.# (CMI28) Digital Ground.*
Pin 25 (CMI332-3) n/c.# (CMI28) CPU Reset switch.*
Pin 26 (CMI332-3) n/c.# (CMI28) Digital Ground.*

Notes:

 # - these connections are on Audio Rack only.

*** - these connections (from the CMI28 board only) are for debugging purposes only. If two push-button switches are connected between pins 23 & 24 and pins 25 & 26, they can be used to manually halt and reset the 68K processor, respectively.**

CMI-333 3.5
SMPTE Module

Introduction

The SMPTE input has a balanced line receiver. The signal is then filtered and converted to TTL compatible signals through the LM311 comparator. The SMPTE out signal is converted from a TTL to a balanced line signal. The SMPTE in and out signals are received and transmitted via two 3-pin XLR sockets.

Pin Connections for the 26-way Connector

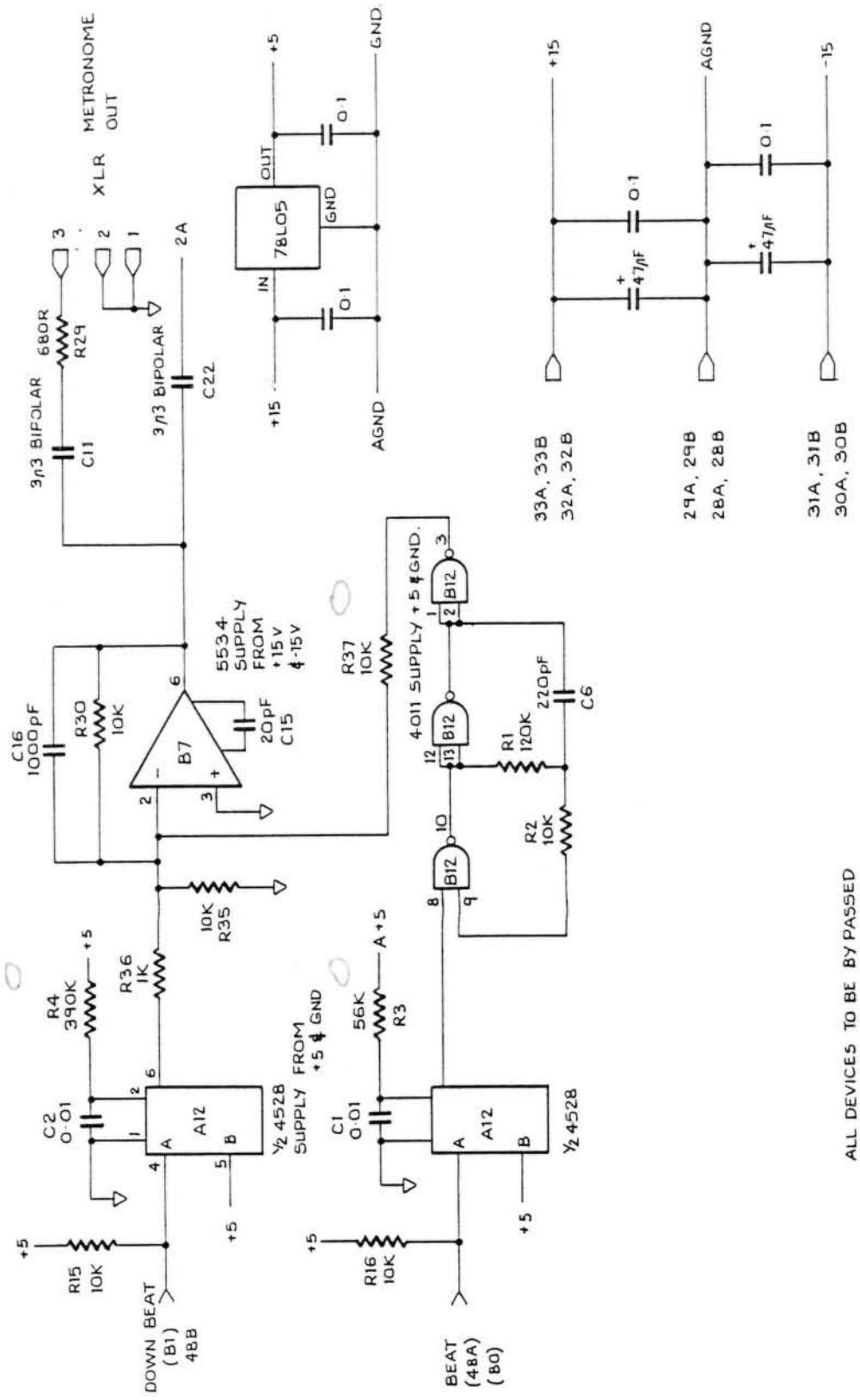
(between the CMI-28 and CMI-332 and CMI-333)

Pin 1 MIDI out A.
Pin 2 +5 volts.
Pin 3 MIDI in A.
Pin 4 SYNC out 1.
Pin 5 MIDI out B.
Pin 6 SYNC out 2.
Pin 7 MIDI in B.
Pin 8 SYNC out 3.
Pin 9 MIDI out C.
Pin 10 Digital Ground.
Pin 11 MIDI in C.
Pin 12 Digital Ground.
Pin 13 MIDI out D.
Pin 14 RESET/START.
Pin 15 MIDI in D.
Pin 16 RUN/STOP.
Pin 17 SMPTE code in.
Pin 18 Digital Ground.
Pin 19 SMPTE code out.
Pin 20 *CLICK* out; *SYNC* out 4.
Pin 21 CLICK in.
Pin 22 (CMI332-3) Analog Ground.# (CMI28) n/c.*
Pin 23 (CMI332-3) +15 volts.# (CMI28) CPU Halt switch.*
Pin 24 (CMI332-3) -15 volts.# (CMI28) Digital Ground.*
Pin 25 (CMI332-3) n/c.# (CMI28) CPU Reset switch.*
Pin 26 (CMI332-3) n/c.# (CMI28) Digital Ground.*

Notes:

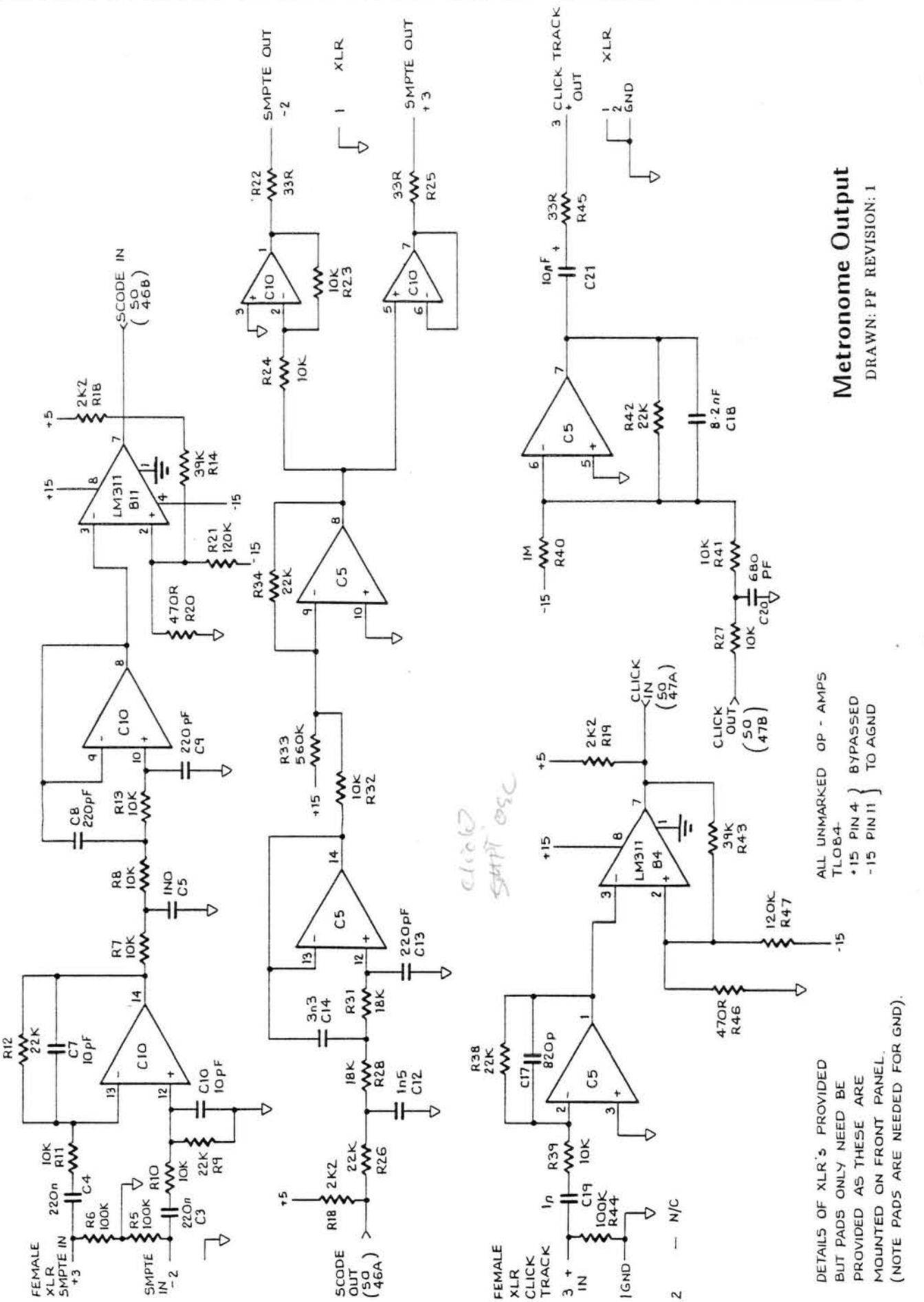
- these connections are on Audio Rack only.

* - these connections (from the CMI28 board only) are for debugging purposes only. If two push-button switches are connected between pins 23 & 24 and pins 25 & 26, they can be used to manually halt and reset the 68K processor, respectively.



SMPTE Drivers and Sockets

DRAWN: PF REVISION: 1


Metronome Output
DRAWN: PF REVISION: 1
SCODE IN (50 46B)
SMPTE OUT -2
SMPTE OUT +3
1 XLR
3 CLICK TRACK + OUT
XLR
1 GND
2 — N/C
FEMALE XLR SMPTE IN +3
SMPTE IN -2
SCODE OUT (50 46A)
FEMALE XLR CLICK TRACK
3 + IN
1 GND
CLICK IN (50 47A)
CLICK OUT (50 47B)
LM311 B11
LM311 B4
C10
C5
ALL UNMARKED OP - AMPS TL084
+15 PIN 4 } BYPASSED
-15 PIN 11 } TO AGND
DETAILS OF XLR'S PROVIDED BUT PADS ONLY NEED BE PROVIDED AS THESE ARE MOUNTED ON FRONT PANEL. (NOTE PADS ARE NEEDED FOR GND).

CMI-334 3.6
Audio Mixer Module

Terminology
AM: Audio Module
AMM: Audio Mixer Module
AR: Audio Rack
AMB: Audio MotherBoard

Introduction
The Audio Mixer Module (AMM) provides a fixed 16 channel into 1 mixing facility for the Audio Rack (AR) assembly. It also provides the latches for controlling the facility to mix the A and B halves of the Audio Modules (AM). It is not essential to the operation of the CMI and may be left out if desired.

Mixing
The signals to be mixed are received as differential analog inputs from each channel. They are buffered and converted into unipolar form before being mixed and again buffered for output on an XLR type connector. This mixed signal is also sent to the CMI310 power supply and headphone amplifier where it is used to drive the headphone output. The output from the mixer to the CMI310 is connected electrically to both slots 10 and 11 of the AMB. If two mixer modules are present then the signal level to the headphones will be mixed but reduced in level. Note that, since the CMI334 is mono, both left and right signals to the headphones are connected together.

Controls
The AMM contains two eight bit latches, level shifters and address decoding logic to provide control signals to each AM. These signals are used to mix the A & B half of the module so that the channel card may pan between each voice.

Buffer Circuitry and Mixing
(refer schematic CMI334-00, 01,02)
The incoming differential signals from each voice are buffered by op-amp D1, D3, D4, D6, D7, D9, D10 and D12. These operate in a standard differential receiver format with some high frequency roll-off and stability provided by the 220pF capacitors.

Mixing is accomplished by the 16 10K ohm resistors feeding into the virtual earth current node of IC B1 pin 2. The 220 ohm standoff resistor provides some isolation from the relatively large capacitive load seen by pin 2. IC B1 is bypassed from pin 1 to 2 by a 470pF ceramic cap which reduces the bandwidth (and hence noise power) and also slugs the amplifier to a gain of 0 at high frequencies. The 1K ohm resistor in series with the 10K give a gain of just over 1 for normal mixing conditions. Switch 1 bypasses the 10K ohm for large signals so that output clipping may be avoided. It can also be used to reduce signal level into mixing consoles or amplifiers with insufficient headroom.

IC B2 is a 5532 type which may directly drive a 600 ohm balanced line in differential form. Note that 33 ohm standoff resistors are included in the feedback path reducing the output impedence while improving the stability with a capacitive load.

Two 1K ohm resistors are fitted to Rev 3 boards and also to Rev 2.1A to allow two mixer modules to be inserted into a CMI without damage. If these resistors are missing then the appropriate FCN should be performed. They are installed in series with the output signal to edge connectors 2 and 3 sides A and B.

Control Circuitry

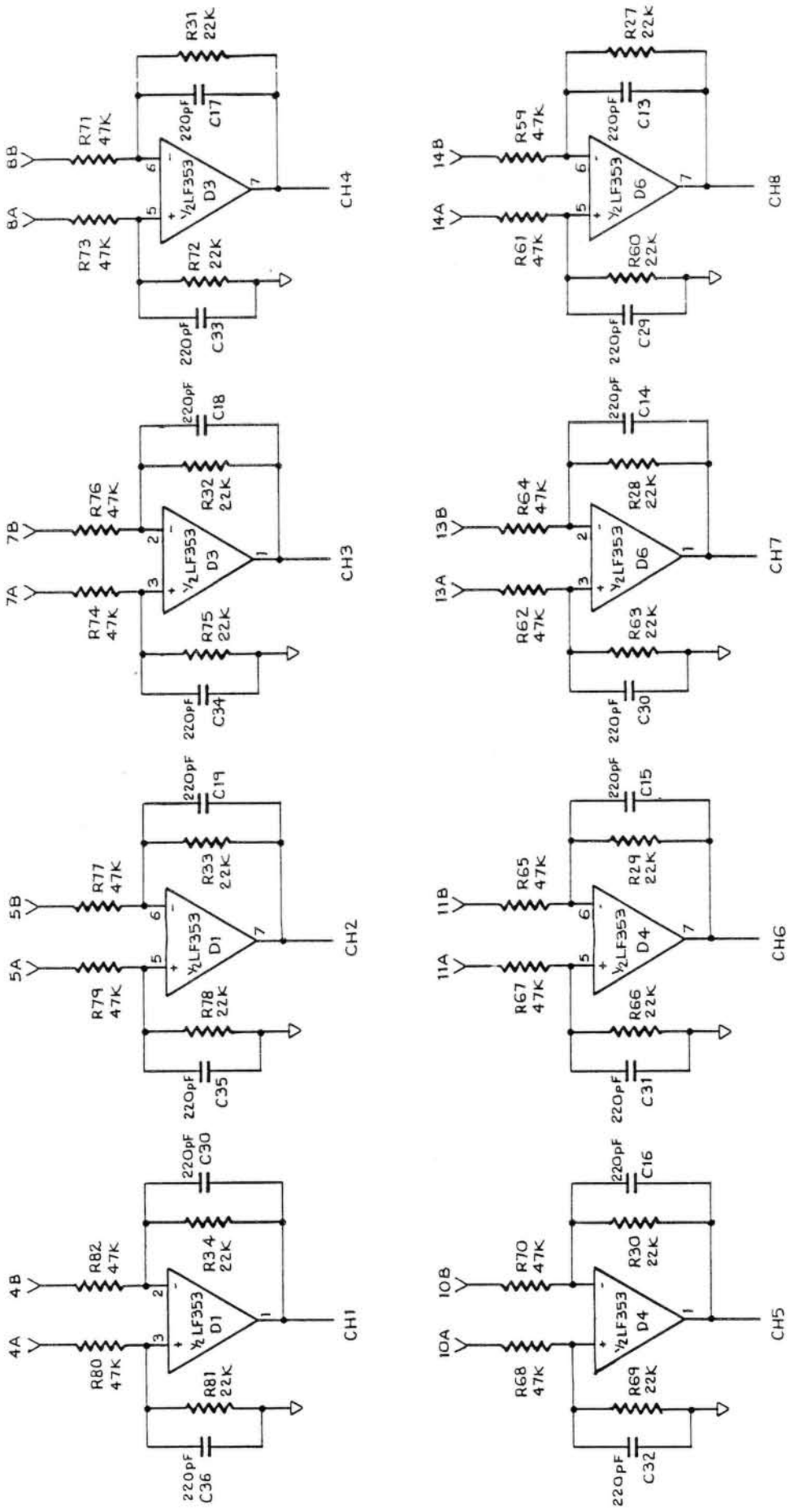
(refer schematic CMI334-03)

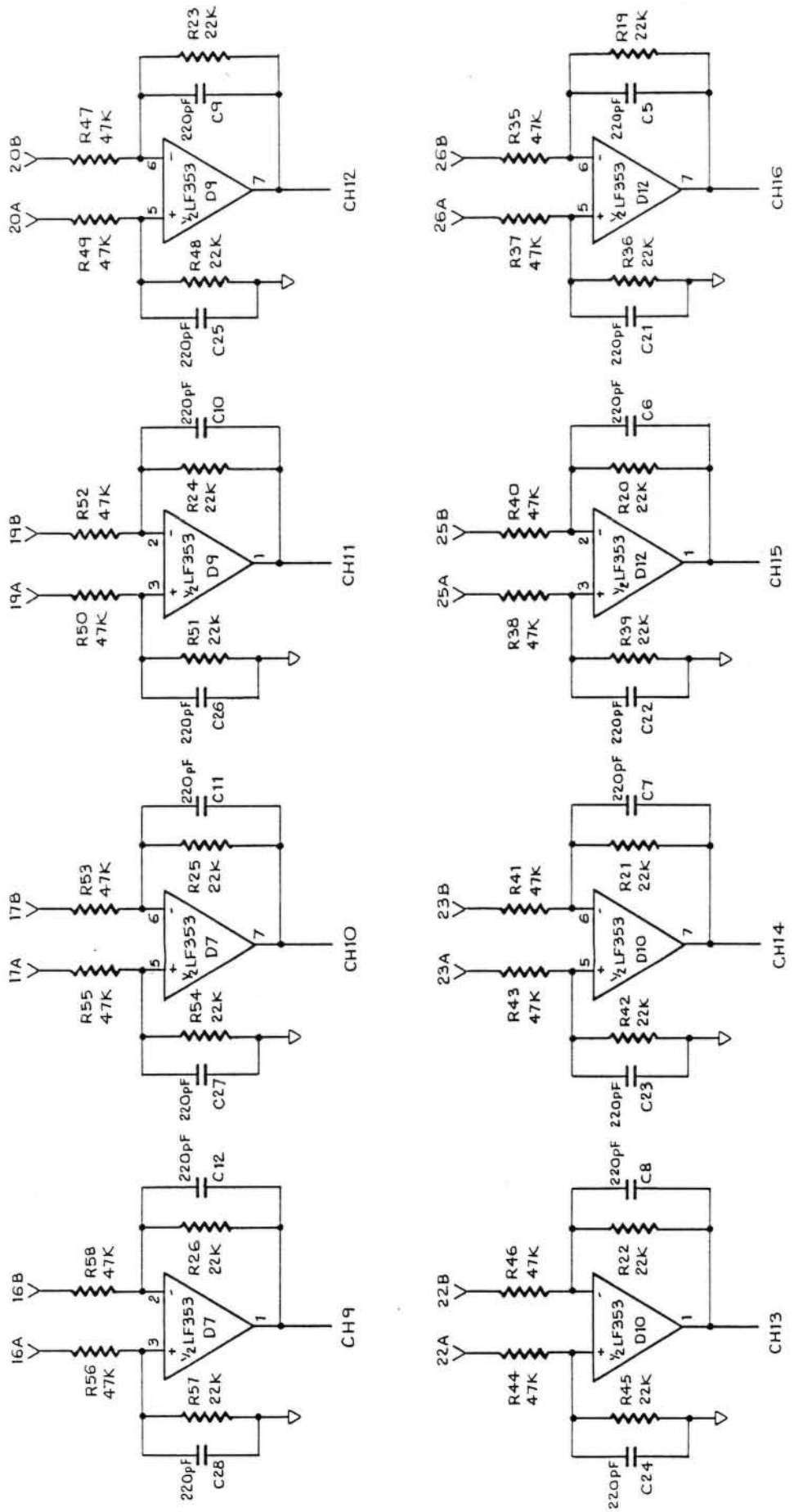
IC A9 (74HC138) decodes the lower address bits from the debug card PIA providing outputs so as to enable the latches (IC's A7 and B7 4099's) when 0 or 8 is presented. These signals and the higher bits are level shifted by IC B9 (4504) and fed to the latches. These further decode the higher bits and latch the state of bit 7 for output to the Audio Modules.

ICs A7 and B7 are bit addressable latches in which bit settings 'map' the PIA data to channel selections for mix control signals.

The LM317T provides the regulated 7 volts for driving the level shifted controls.

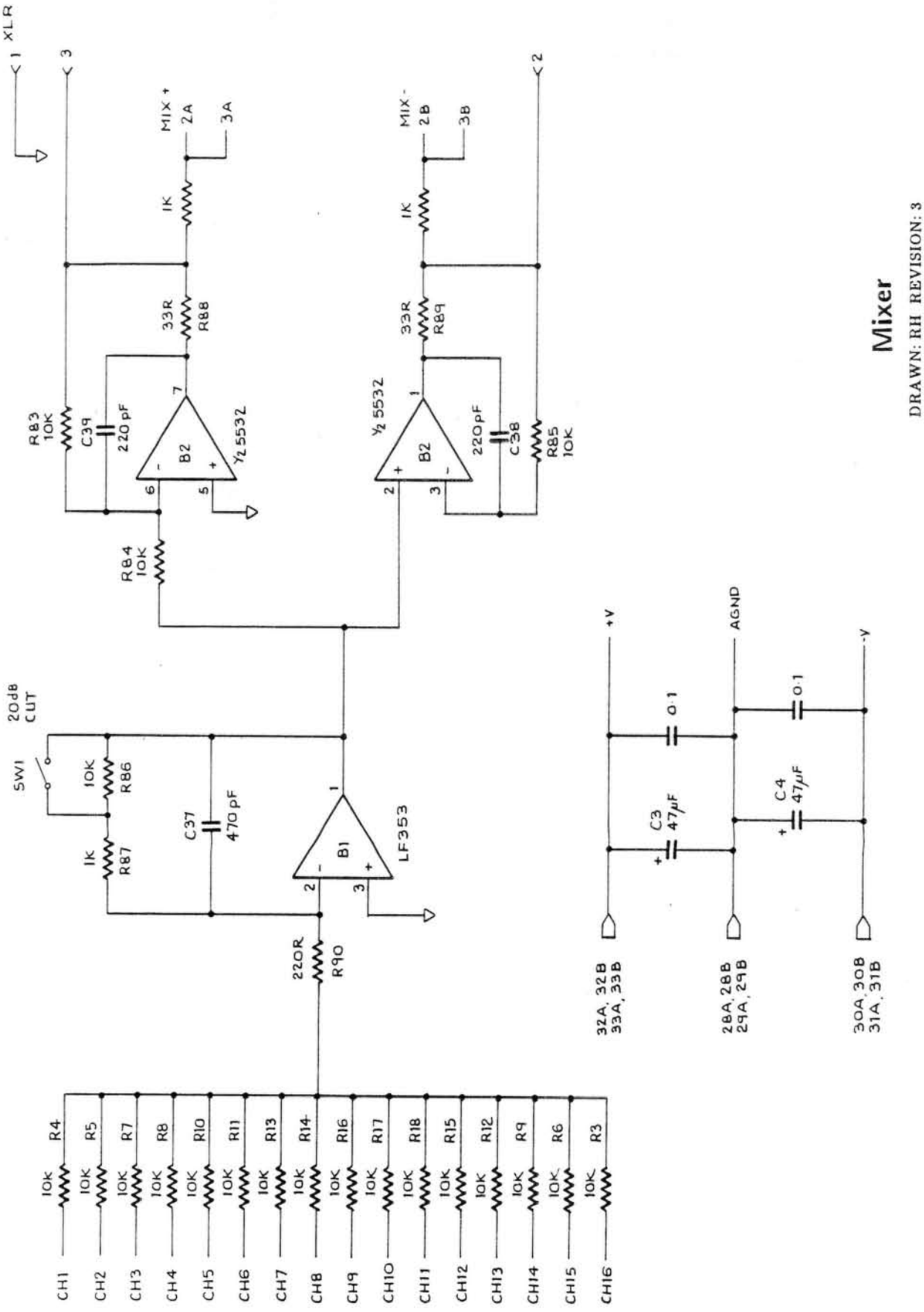
The rev 3 circuit card differs only in that it has sixteen LEDs added and a 16 pin socket for ease of testing the control circuitry. The LEDs indicate a control line is active.


Differential Receivers
DRAWN: RH REVISION: 3
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
½LF353
D1
D3
D4
D6
4A
4B
5A
5B
7A
7B
8A
8B
10A
10B
11A
11B
13A
13B
14A
14B
R80 47K
R82 47K
R79 47K
R77 47K
R74 47K
R76 47K
R73 47K
R71 47K
R67 47K
R65 47K
R62 47K
R64 47K
R61 47K
R59 47K
R68 47K
R70 47K
R81 22K
R34 22K
R78 22K
R33 22K
R75 22K
R32 22K
R72 22K
R31 22K
R69 22K
R30 22K
R66 22K
R29 22K
R63 22K
R28 22K
R60 22K
R27 22K
220pF C36
220pF C30
220pF C35
220pF C19
220pF C34
220pF C18
220pF C33
220pF C17
220pF C32
220pF C16
220pF C31
220pF C15
220pF C30
220pF C14
220pF C29
220pF C13



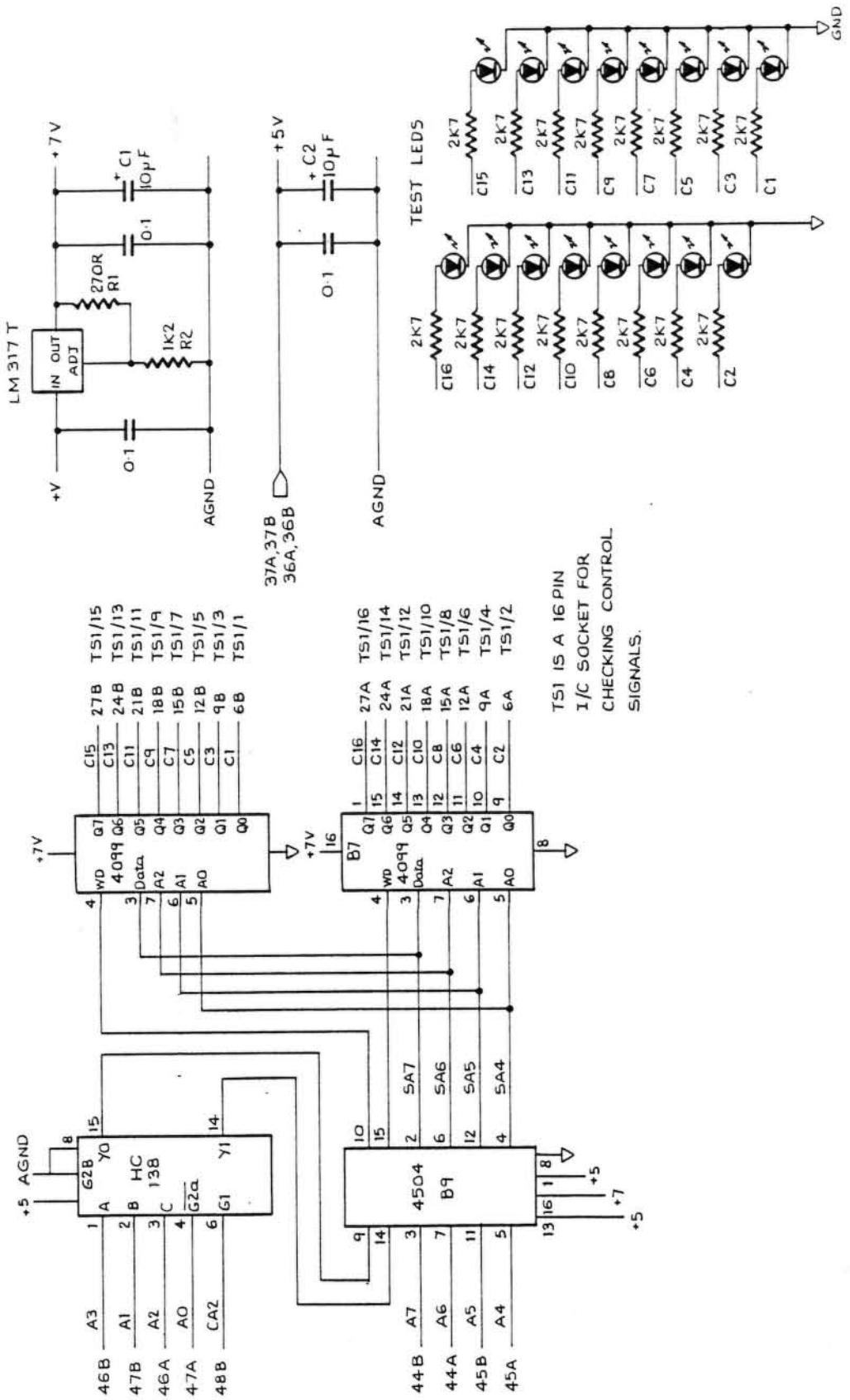
Differential Receivers

DRAWN: RH REVISION: 3



Mixer

DRAWN: RH REVISION: 3


Control Circuitry
DRAWN: RH REVISION: 3
TEST LEDS
GND
+7V
+5V
LM 317 T
IN OUT ADJ
270R R1
1K2 R2
+C1 10µF
+C2 10µF
0·1
AGND
+V
37A,37B
36A,36B
2K7
C16 C14 C12 C10 C8 C6 C4 C2
C15 C13 C11 C9 C7 C5 C3 C1
TS1 IS A 16 PIN I/C SOCKET FOR CHECKING CONTROL SIGNALS.
4099 Data
B7
B9
HC 138
4504
TS1/15 TS1/13 TS1/11 TS1/9 TS1/7 TS1/5 TS1/3 TS1/1
TS1/16 TS1/14 TS1/12 TS1/10 TS1/8 TS1/6 TS1/4 TS1/2
27B 24B 21B 18B 15B 12B 9B 6B
27A 24A 21A 18A 15A 12A 9A 6A
SA7 SA6 SA5 SA4
A3 A1 A2 A0 CA2
A7 A6 A5 A4
46B 47B 46A 47A 48B
44B 44A 45B 45A

CMI-335 3.7
Audio Mother Board

Terminology
WB: Waveform Buss
WP: Waveform Processor CMI-33
WRAM: Waveform RAM (1 to 7 cards each 2Mbytes) CMI39
CC: Channel Card (8 used per system) CMI31
CSC: Channel Support Card CMI32
AM: Audio Module (8 cards used per system) CMI-331
AMM: Audio Mixer Module CMI-334
MIDI CARD: CMI-332
SMPTE CARD: CMI-333
SAMPLER: CMI-337
SHIELD: CMI-336
DEBUG CARD: Q133
SMIDI BOARD: CMI28
AMB: Audio MotherBoard

Introduction

The Audio MotherBoard (AMB) is the central interface between the digital part or computer of the CMI and the audio output stage.

The audio circuitry receives all its power supplies and signals from this card. The exception is, of course, the Audio outputs and the MIDI, SMPTE and Sampler interfaces to the outside world.

The AMB is located in the centre of the CMI facing in the opposite direction to the Digital motherboard.

Structure of the Motherboard

The AMB is structured so that most connections of audio signals are accomplished without the need for hand wiring as in the Series II machines. The board is set up with thirteen slots into which plug the various modules for interfacing to the outside world. A modular arrangement was used to allow the required equipment to fit while still allowing ease of servicing and upgradeability. The power supply from CMI310 is via a multi-way power cable soldered directly to the board. The digital five volts is connected directly from the digital motherboard to the five volt buss on rev 0, 1 and 2 boards while rev 3 and 4 have a five amp fuse mounted on the AMB and solder pads for the cables.

Starting at the right hand end of the AMB is slot 1 which holds the Sampler card for stereo input. The next eight slots are for the eight Audio Modules (AM) followed by two slots (10 & 11) for mixer modules and two for the MIDI and SMPTE modules (12 & 13).

Cables to supply these cards are connected via IDC type mass termination connectors at either end of the AMB.

The digital and analog grounds have their only direct connection on the CMI-335 between slots 5 and 6. Both grounds are separately bussed to each slot.

Interconnection Structure

Slot 1 (Sampler CMI-337) is connected to its own power supply from CMI310 via the power cable, signals are connected via a ten way cable to the Waveform Processor (WP).

Slots 2 through 9 are for Audio Modules. The Audio Modules connect to the motherboard via two edge connectors, one a double

sided thirty-four way device (68 pins total) for those signals which are bussed along the motherboard and the second a double sided thirteen way connector (26 pins total). This connector is an edge to cable IDE type connector which allows the signals from the CC to connect directly to the AM without going via the AMB first. Since the two connectors are in line with one another they are considered to be one edge connector split into two sections. This allows unambiguous labelling of the AM edge fingers. To satisfy the physical positioning of the two edge connectors the same numbering pattern used in the digital card cage is used here, i.e. The edge connector is numbered as if it were a 78 way double sided device with the solder side labelled as the A side and the component side as the B side, the IDE type connector occupying fingers 8 A and B through to 20 A and B, the 34 way connector then occupies fingers 45 A and B through to 78 A and B.

The above numbering system is used everywhere with any exception specifically noted.

The AM slots receive data, power and digital control lines and output audio for mixing purposes via the 34 way connector. The flat ribbon cable connected to the IDE connector carries power from the AM to the CC, data clocks, and analog control voltages in the reverse direction.

Slots 10 and 11 are for mixer modules which are optional devices. Each CMI is shipped with a CMI-334 basic mixer module which is primarily for headphone and monitoring purposes. Slots 10 and 11 differ in that the control function outputs from the mixer modules are connected on slot 11 but not on slot 10. Two reasons exist for this, one is that if two modules are inserted then both would conflict on driving the mixer lines, the second reason is that by positioning the mixer in slot 10 the AMs are set so that no digital control signals (i.e. mix) are active.

Slots 12 and 13 are for the MIDI and SMPTE support modules. These may be inserted in any order since these slots have no electrical difference. The MIDI and SMPTE cards, and the mixers, connect via a double sided 48 way edge connector (96 pins). The main connections are to the CMI-28 SMIDI card and to the power supply. Note that the MIDI connection to the FAIRLIGHT music keyboard is routed in an unusual fashion, this is to avoid additional cabling within the CMI.

Circuit Description

The AMB is mainly an interconnection device for various signals used in the audio section.

Looking from the component side, in the top left corner the 34 way flat cable connector which carries the 16 bit data from the waveform buss in differential form is located. This data is bussed along slots 2 through 9 for the AMs. The 10 way ribbon cable connector, located at the bottom right corner of the AMB near slot 1, is for the Sampler signals to the waveform processor.

On the left hand end of the AMB are 3 ribbon cable connectors, the Debug cable (J1) , the MIDI cable (J2) and the headphone output cable (J3). These connect to the Debug card, the MIDI card and the CMI310 power supply board respectively.

Slot Schedule

Each slot is listed below showing the connections available from the AMB.

Slot 1: Stereo ADC.

Side A

Pin	Signal Name	Function	Source
20	MUTE	power on mute	various
17	-DATA	data from WP	CMI33
16	+DATA	data from WP	CMI33
15	-SAMPCLK	start conversion pulse	CMI33
14	+SAMPCLK	start conversion pulse	CMI33
13	DATAOUT	data to WP	CMI337
12	CLKOUT	bit clock to WP	CMI337
11	EOC	end of conversion	CMI337
9,10	DSGND	digital gnd	CMI337
7,8	+9V	+9V sampler supply	CMI310
5,6	-20V	-20V sampler supply	CMI310
3,4	ASGND	sampler analog gnd	CMI310
1,2	+20V	+20V sampler supply	CMI310

Side B

Pin	Signal Name	Function	Source
9,10	DSGND	digital gnd	CMI33
7,8	+9V	+9 sampler supply	CMI310
5,6	-20V	-20V sampler supply	CMI310
3,4	ASGND	sampler analog gnd	CMI310
1,2	+20V	+20 sampler supply	CMI310

A polarising key is fitted in place of fingers 39A and B

Slots 2 to 9
These signals are bussed.
Please see text for description of numbering system used for edge fingers.

Side A

Pin	Signal Name	Function	Source
77,78	D+5	digital 5 volts	CMI35
76-61	D0+ to D15+[1]	16 bit WB data +	CMI32
59,60	DGND	digital gnd	CMI35
58		polarizing key	
56,57		spare	
55	MUTE	mute control	various
53,54	+15V	regulated +15volts	CMI310
51,52	-15V	regulated -15volts	CMI310
48-50	AGND	analog gnd	CMI310

Note 1: data to the audio modules is differential with + and - on opposite sides of the edge connector.

The following are signals which arrive at slots 2 through 9 via IDE type cable to edge connectors, each CC connecting to its corresponding AM (slot 2 from CC 1,.. slot 9 from CC 8).

20	n/c	no connection	CMI31
19	DGND	digital gnd	CMI31
18	PCLK-2[2]	pitch clock 2	CMI31
17	PCLK-1[2]	pitch clock 1	CMI31
16	DCLK-1[2]	data clock 1	CMI31
15	DCLK-2[2]	data clock 2	CMI31
13,14	n/c	no connection	CMI31
12	AGND	analog gnd	CMI331
11	+15V	+15volts to CMI31	CMI331
10	RES1[3]	resonance control	CMI31
9	VCF1[3]	filter control	CMI31
8	VCA1[3]	VCA control	CMI31

Note 2: PCLKs and DCLKs are differential with + and - on opposite sides of the connector. Two differential pairs of each for two channels on the AM.
Note 3: Two sets of RES, VCF and VCA on opposite sides of the connector for the Two channels of the AM.

Side B

Pin	Signal Name	Function	Source
77,78	D+5	digital +5 volts	CMI35
76-61	D0- to D15-[1]	data 0 to data 15 -	CMI32
59,60	DGND	digital gnd	CMI35
58		polarizing key	
55-57		spare	
53,54	+15V	regulated +15 volts	CMI310
51,52	-15V	regulated -15 volts	CMI310
48-50	AGND	analog gnd	CMI310

The following are signals which arrive at slots 2 through 9 via IDE cable to edge connectors, each CC connecting to its corresponding AM (slot 2 from CC 1,.. slot 9 from CC 8).

20	n/c	no connection	CMI31
19	n/c	no connection	CMI31
18	DGND	digital gnd	CMI31
17	PCLK+2[2]	pitch clock	CMI31
16	PCLK+1[2]	pitch clock	CMI31
15	DCLK+1[2]	data clock	CMI31
14	DCLK+2[2]	data clock	CMI31
13	n/c	no connection	CMI31
12	-15V	-15volts to CMI31	CMI331
11	AGND	analog gnd to CMI31	CMI331
10	RES2[3]	resonance control	CMI31
9	VCF2[3]	filter control	CMI31
8	VCA2[3]	VCA control	CMI31

Signals which are not common or bussed are described below.

Slot 2 — Audio Module 1

Side A

Pin	Signal Name	Function	Source
47	CONTROL1	audio module control 1	slot 11
46	AUDIO1+	channel 1 audio +	CMI331
45	AUDIO2+	channel 2 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL2	audio module control 2	slot 11
46	AUDIO1-	channel 1 audio -	CMI331
45	AUDIO2-	channel 2 audio -	CMI331

Slot 3 — Audio Module 2

Side A

Pin	Signal Name	Function	Source
47	CONTROL3	audio module control 3	slot 11
46	AUDIO3+	channel 3 audio +	CMI331
45	AUDIO4+	channel 4 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL4	audio module control 4	slot 11
46	AUDIO3-	channel 3 audio -	CMI331
45	AUDIO4-	channel 4 audio -	CMI331

Slot 4 — Audio Module 3

Side A

Pin	Signal Name	Function	Source
47	CONTROL5	audio module control 5	slot 11
46	AUDIO5+	channel 5 audio +	CMI331
45	AUDIO6+	channel 6 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL6	audio module control 6	slot 11
46	AUDIO5-	channel 5 audio -	CMI331
45	AUDIO6-	channel 6 audio -	CMI331

Slot 5 — Audio Module 4

Side A

Pin	Signal Name	Function	Source
47	CONTROL7	audio module control 7	slot 11
46	AUDIO7+	channel 7 audio +	CMI331
45	AUDIO8+	channel 8 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL8	audio module control 8	slot 11
46	AUDIO7-	channel 7 audio -	CMI331
45	AUDIO8-	channel 8 audio -	CMI331

Slot 6 — Audio Module 5

Side A

Pin	Signal Name	Function	Source
47	CONTROL9	audio module control 9	slot 11
46	AUDIO9+	channel 9 audio +	CMI331
45	AUDIO10+	channel 10 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL10	audio module control 10	slot 11
46	AUDIO9-	channel 9 audio -	CMI331
45	AUDIO10-	channel 10 audio -	CMI331

Slot 7 — Audio Module 6

Side A

Pin	Signal Name	Function	Source
47	CONTROL11	audio module control 11	slot 11
46	AUDIO11+	channel 11 audio +	CMI331
45	AUDIO12+	channel 12 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL12	audio module control 12	slot 11
46	AUDIO11-	channel 11 audio -	CMI331
45	AUDIO12-	channel 12 audio -	CMI331

Slot 8 Audio Module 7

Side A

Pin	Signal Name	Function	Source
47	CONTROL13	audio module control 13	slot 11
46	AUDIO13+	channel 13 audio +	CMI331
45	AUDIO14+	channel 14 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL14	audio module control 14	slot 11
46	AUDIO13-	channel 13 audio -	CMI331
45	AUDIO14-	channel 14 audio -	CMI331

Slot 9 Audio Module 8

Side A

Pin	Signal Name	Function	Source
47	CONTROL15	audio module control 15	slot 11
46	AUDIO15+	channel 15 audio +	CMI331
45	AUDIO16+	channel 16 audio +	CMI331

Side B

Pin	Signal Name	Function	Source
47	CONTROL16	audio module control 16	slot 11
46	AUDIO15-	channel 15 audio -	CMI331
45	AUDIO16-	channel 16 audio -	CMI331

Slot 10 and 11 **Mixers**
The following signals are common to both slots.

Side A

Pin	Signal Name	Function	Source
48	CA1	Debug PIA line	Q133
47	A0	Debug PIA line	Q133
46	A2	Debug PIA line	Q133
45	A4	Debug PIA line	Q133
44	A6	Debug PIA line	Q133
43	B0	Debug PIA line	Q133
42	B2	Debug PIA line	Q133
41	B4	Debug PIA line	Q133
40	B6	Debug PIA line	Q133
39		Polarizing key	
38	CB1	Debug PIA line	Q133
36,37	D+5	digital +5 volts	CMI35
34,35	DGND	digital gnd	CMI35
32,33	+15V	regulated +15 volts	CMI310
30,31	-15V	regulated -15 volts	CMI310
28,29	AGND	analog gnd	CMI310
27	CONTROL16	control line 16	CMI334
26	AUDIO16+	audio output 16	slot 9
25	AUDIO15+	audio output 15	slot 9
24	CONTROL14	control line 14	CMI334
23	AUDIO14+	audio output 14	slot 8
22	AUDIO13+	audio output 13	slot 8
21	CONTROL12	control line 12	CMI334
20	AUDIO12+	audio output 12	slot 7
19	AUDIO11+	audio output 11	slot 7
18	CONTROL10	control line 10	CMI334
17	AUDIO10+	audio output 10	slot 6
16	AUDIO9+	audio output 9	slot 6
15	CONTROL8	control line 8	CMI334
14	AUDIO8+	audio output 8	slot 5
13	AUDIO7+	audio output 7	slot 5
12	CONTROL6	control line 6	CMI334
11	AUDIO6+	audio output 6	slot 4
10	AUDIO5+	audio output 5	slot 4
9	CONTROL4	control line 4	CMI334
8	AUDIO4+	audio output 4	slot 3
7	AUDIO3+	audio output 3	slot 3
6	CONTROL2	control line 2	CMI334
5	AUDIO2+	audio output 2	slot 2
4	AUDIO1+	audio output 1	slot 2
3	MIXRT+	right mixed audio	CMI334
2	MIXLFT+	left mixed audio	CMI334

Side B

Pin	Signal Name	Function	Source
48	CA2	debug PIA line	Q133
47	A1	debug PIA line	Q133
46	A3	debug PIA line	Q133
45	A5	debug PIA line	Q133
44	A7	debug PIA line	Q133
43	B1	debug PIA line	Q133
42	B3	debug PIA line	Q133
41	B5	debug PIA line	Q133
40	B7	debug PIA line	Q133
39		polarizing key	
38	CB2	debug PIA line	Q133
36,37	D+5	digital 5 volts	CMI35
34,35	DGND	digital GND	CMI35
32,33	+15V	regulated supply	CMI310
30,31	-15V	regulated supply	CMI310
28,29	AGND	analog GND	CMI35
27	CONTROL15	control line 15	CMI334
26	AUDIO16-	audio output 16	slot 9
25	AUDIO15-	audio output 15	slot 9
24	CONTROL13	control line 13	CMI334
23	AUDIO14-	audio output 14	slot 8
22	AUDIO13-	audio output 13	slot 8
21	CONTROL11	control line 11	CMI334
20	AUDIO12-	audio output 12	slot 7
19	AUDIO11-	audio output 11	slot 7
18	CONTROL9	control line 9	CMI334
17	AUDIO10-	audio output 10	slot 6
16	AUDIO9-	audio output 9	slot 6
15	CONTROL7	control line 7	CMI334
14	AUDIO8-	audio output 8	slot 5
13	AUDIO7-	audio output 7	slot 5
12	CONTROL5	control line 5	CMI334
11	AUDIO6-	audio output 6	slot 4
10	AUDIO5-	audio output 5	slot 4
9	CONTROL3	control line 3	CMI334
8	AUDIO4-	audio output 4	slot 3
7	AUDIO3-	audio output 3	slot 3
6	CONTROL1	control line 1	CMI334
5	AUDIO2-	audio output 2	slot 2
4	AUDIO1-	audio output 1	slot 2
3	MIXRT-	right mixed audio	CMI334
2	MIXLFT-	left mixed audio	CMI334
1	MUTE	mute control line	various

The following signals are unique to each slot.

Slot 10
Side A

Pin	Signal Name	Function	Source
1	D+5	module select 2	CMI35

Slot 11

Pin	Signal Name	Function	Source
1	DGND	module select 1	CMI35

Slot 12 and 13 MIDI and SMPTE
Both slots are identical.

Side A

Pin	Signal Name	Function	Source
47	CLICK IN	click track input	CMI333
46	SMPTE OUT	SMPTE signal output	CMI28
45	RUN/STOP	drum machine control	CMI28
44	RESET/START	drum machine control	CMI28
43	MIDI IN C	MIDI input 3	CMI332
42	SYNC OUT 3	sync output	CMI28
41	SYNC OUT 2	sync output	CMI28
40	SYNC OUT 1	sync output	CMI28
39	MIDI OUT A	MIDI output 1	CMI28
36,37	D+5	digital 5 volts	CMI35
34,35	DGND	digital GND	CMI35
32,33	+15V	regulated supply	CMI310
30,31	-15V	regulated supply	CMI310
28,29	AGND	analog GND	CMI310
21	LK19	link between slots	future
20	LK17	link between slots	future
19	LK15	link between slots	future
18	LK13	link between slots	future
17	LK11	link between slots	future
16	LK9	link between slots	future
15	LK7	link between slots	future
14	LK5	link between slots	future
13	LK3	link between slots	future
12	LK1	link between slots	future
10		polarizing key	
3	MUTE	mute control line	various
2	METOUT	metronome out	CMI333
1	KEY+	MIDI from keyboard	CMI310