Digital Card Cage 2

CP.

Contents

Q209 2.2

Dual 6809 Central Processor

Introduction

The Q209 contains the dual 6809 processors , on board processor communication hardware entailing indivisible instructions, processor readable identification / map state , interprocessor interrupts, automatic map switching FUSE register and hardware trace logic to enable single stepping for software debugging.

The Dual Processor card multiplexes each processor onto a common address and data buss in an interleaved manner, each processor therefore may simultaneously access the same memory location without any contention, if the memory is mapped onto both processors. (See Q256 functional description)

The memory addresses are issued to the buss 225 nanoseconds prior to the access cycle, allowing addresses to be mapped by the memory card, to allow for accessing greater than 64K of RAM.

Many global timing signals are issued from the processor for general buss control .

Master Timing Signals

(refer schematic Q209-00)

All system timing signals are derived from crystal-controlled 40MHz oscillator Q1. Flip-flop 10F derives two opposite phase 20 MHz square waves. Quad D-type latch D2, together with the NAND gate in 7F, forms a 10 state Johnson, or twisted-tail ring counter. Each state is of 50ns duration. The system signals are decoded by NAND gates in 8E from the output of this counter.

Dynamic Memory Timing Signals

(refer schematic Q209-00)

Four non-inverting buffers of 10A are driven by latch E1 to provide CAS(Column Address Strobe), RAS (Row Address Strobe), CA (Column Address , active low) and RA (Row Address, active low). RAS is delayed relative to CAS by about 20ns by the propagation delay of 11E. RA and CA are complementary.

Data and Address Buss Multiplexing

(refer schematic Q209-03)

Flip-flop 6F , along with associated gating, generates the 6809's E signals. The system address buss is multiplexed by the ADDRESS signals ADD1 and ADD2 , (active low). One-of-four decoders 3E and 4E are used to enable the appropriate address and data buffers, to perform the multiplexing. The data buffer enable signals WRITE1, WRITE2, READ1, READ2 are generated by logical combinations of R/W , VMA , processor phase 2 and DMA lines. The address buss is actually multiplexed 4 ways, as the vectored interupt system may also acquire the buss' least significant bits of the address buss for either processor's vector fetch cycle. The address buffer enables are a function of the Address signal and the Interupt acknowledge.

Phase 2 reference and Address references for each Processor are feed to the buss via buss drivers.

Interrupt Strobe Generation
(refer schematic Q209-02)

Dual D-type flip-flop 9D and 3-input AND gate 8D feed Interrupt Strobe pulses to the buss. These are used by the Priority Interrupt Control Units (PICUs) used to provide vectored interrupts, and also to strobe the vector address latches 8A and 9A. The PICUs are located on the Q133 card. These signals strobe the priority latches continuously, until an interrupt is acknowledged. In this way the Interrupt Priority is maintained at its latest level regardless of delay between an interrupt request being received by the PICU and the associated vector-fetch cycle being executed.

Direct Memory Access
(refer to drawing Q209-00)

DMA requests for each processor are clocked into flip-flop 11D on the falling edge of the phase 2 signal of the respective processor. DMA acknowledge is sent to the buss via buffers and drive signals to the processors are suspended in the phase 1 state for the duration of the DMA cycle. The maximum permissible DMA duration is 5 microseconds. Worst-case DMA latency is 1 microsecond. Latency is the time required to service the request.

Vector-Fetch Decoders
(refer to drawing Q209-01)

The vector state of the processors are decoded by the one-of-four decoders, 2D and NOR gates in 1D. These correspond to addresses in the range FFF0 to FFFF. They correspond to the processor fetching vectors FIRQ, NMI, SWI1, SWI2, SWI3, IRQ and RESTART. The Restart vectors come from ROM so when this is sensed the ROM is enabled and the ram disabled. This is achieved by the ROMEN signal on buss pin 44. On detection of an Interrupt Request vector address from the processor, decoder 2D causes the normal address buss drivers for bits 1 to 4 to be disabled and the Interrupt Address buffers to be enabled in lieu.

Processor System Control

These general functions are controlled through ports at the following locations ...

$FC5E	Indivisible instructions	read
$FC5E	Various CPU functions	write
$FC5F	Map status and CPU ID	read
$FC5F	Automatic map switching FUSE	write

The ID can be read to determine the status of the memory map switching hardware. The CPU ID bit can be read by the CPU to find out which CPU is running the program.
The bits are defined as

D0	CPU ID 0=P1 1=P2
D1	P1 map status 0=map B, 1=map A
D2	P2 map status
D3	zero
D4	n/c (indeterminate)
D5	n/c
D6	n/c
D7	n/c

The "Various CPU functions" is an 8 bit register in which each bit may be independently written to. This register is at location 6D, and it is decoded by devices at 9B and 7A. When written to, the bit address is selected by the 3 least significant bits of the data byte. The state of data bit 3 determines whether the bit is set or cleared.

The four functions provided per processor from this register are:-

0+P interprocessor interrupt
2+P hardware trace
4+P map switch select
6+P fast interrupt request

where P is "0" for processor 1 and "1" for processor 2

Fast interrupts may be generated either by an external signal or from the bus. The on-card FIRQ must be reset by the processor concerned, by writing a reset bit to the register.

Automatic Map Switching

(refer schematic Q209-02)

The memory cards support hardware selectable memory maps. The processors can control the A/$\overline{B}$ select lines, allowing automatic switching between "user(B)" and "system(A)" maps.

Whenever an interrupt or processor restart occurs , the A map will be automatically selected. During an interrupt, the switching will occur after the registers are stacked and before the interrupt vector is fetched.

A FUSE location is provided which causes the map to be switched after a specified number of CPU clock cycles have elapsed. These counters are at 8C for CPU1 and 9C for CPU2. The data written to these counters is buffered by the buffer at 7C. The map changed to is determined by the value of the map switch select bit. The map switch will occur after the Nth CPU cycle after the FUSE register write. The delay is required so that a known number of instructions can be executed for house keeping before the CPU's memory is swapped.

Hardware also selects the A map whenever DMA occurs.

Hardware Trace

An NMI may be generated after each instruction execution for software debugging. This is done by flip-flops 5D and half of AND gate 4F. This function is enabled under software, by access to $FC5E.

Enabling this function inverts the NMI signal from the front panel, so that if the trace hardware is left in the triggered state, front panel NMI requests will still be recognized, but on the opposite edge (since NMI is an edge triggered input).

Indivisible Instructions

(refer to schematic Q209-00)

For the test-and-set and double byte load/store instructions to be effective, the processor not executing the instruction must not be able to alter the flag memory location in question. To this end, the execution of these read/modify/write instructions effectively hangs the other processor for its duration, thus preventing race conditions .

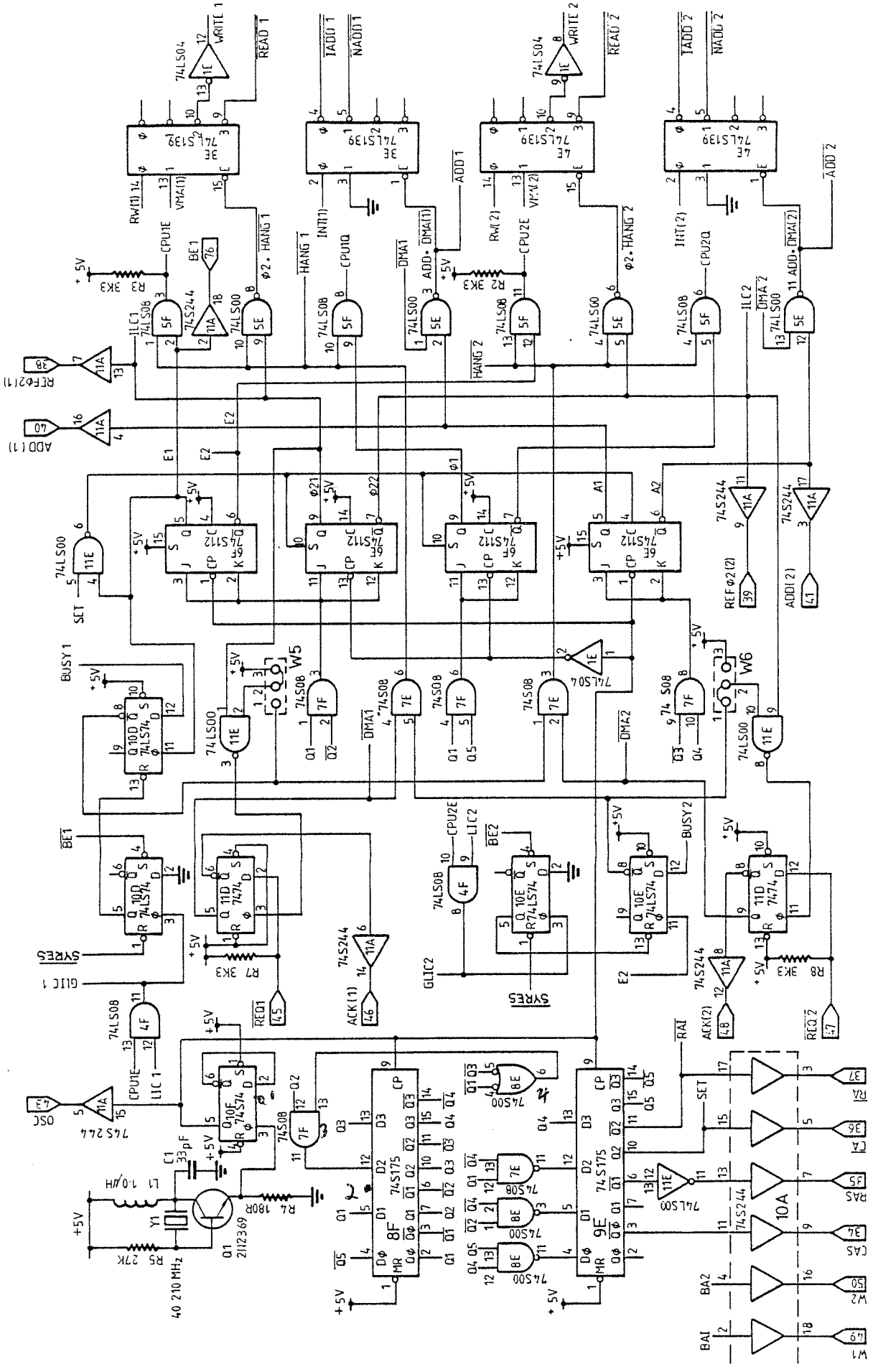
This is achieved by flip-flops 10D, 10E, associated gating and the BUSY outputs from the processors. The BUSY outputs are active when the test and set instruction is executed , and the other processors clock is stopped for its cycle, in the same manner as for DMA transfers. The flip-flops asociated with this are reset at power on to enable the clocks to the 6809's to allow them to be internally reset, at power on reset. To enable this function the instruction to be made indivisible must be immediately preceded by a read from hardware location $FC5E. No interrupt must be allowed to occur between the read and the instruction. This function is automatically disabled at the end of the instruction following the read.

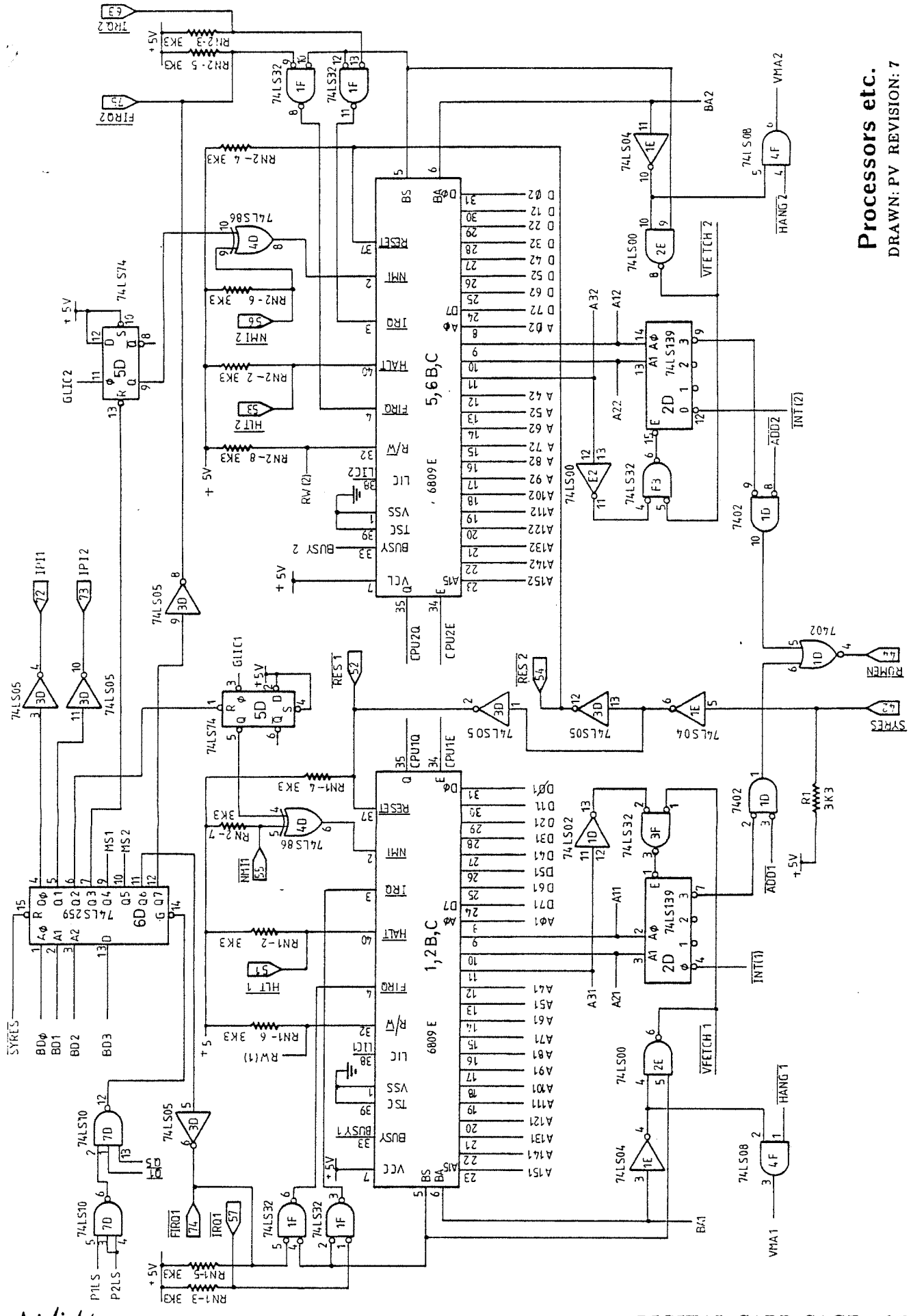
Link Options

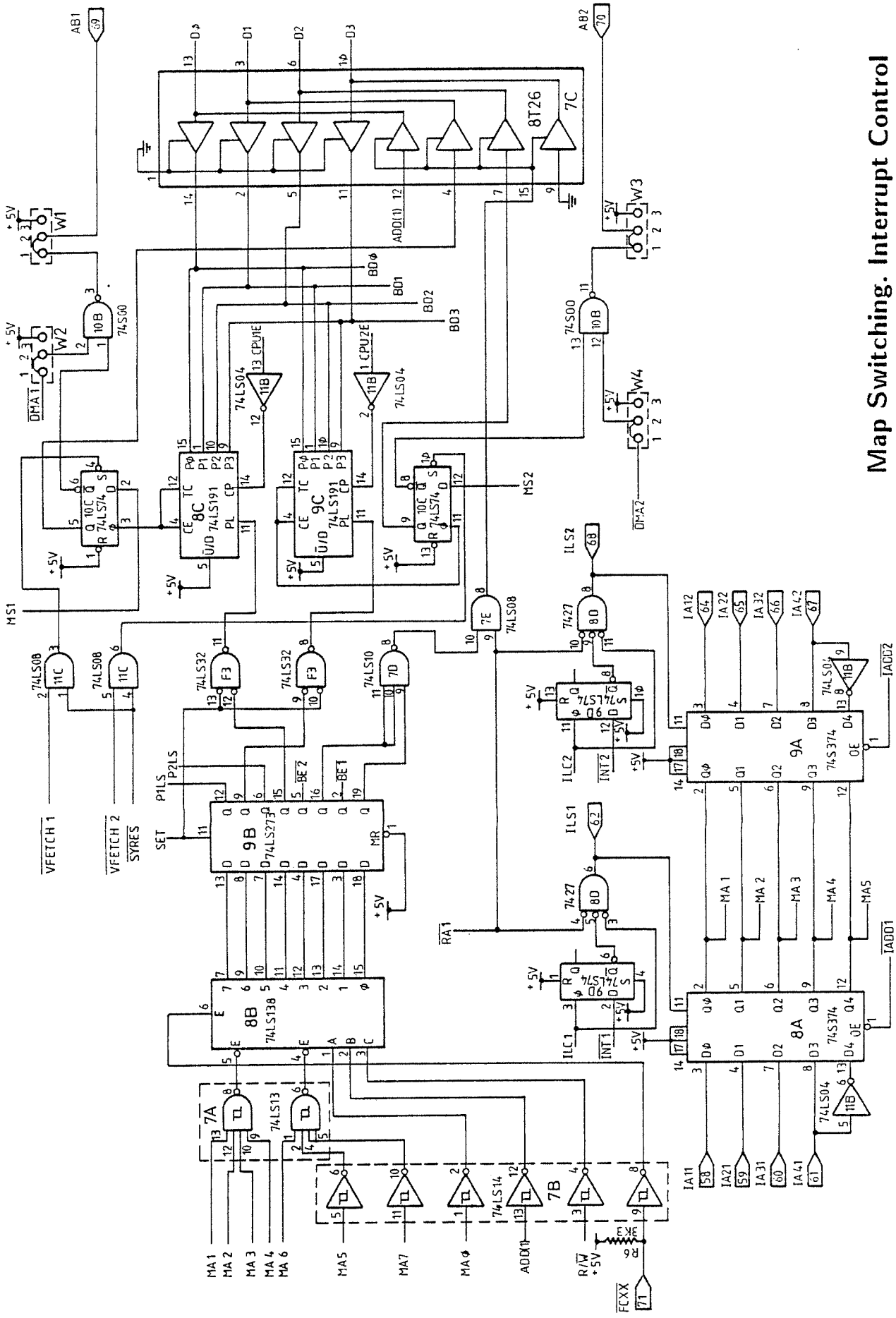
The links have the following functions:

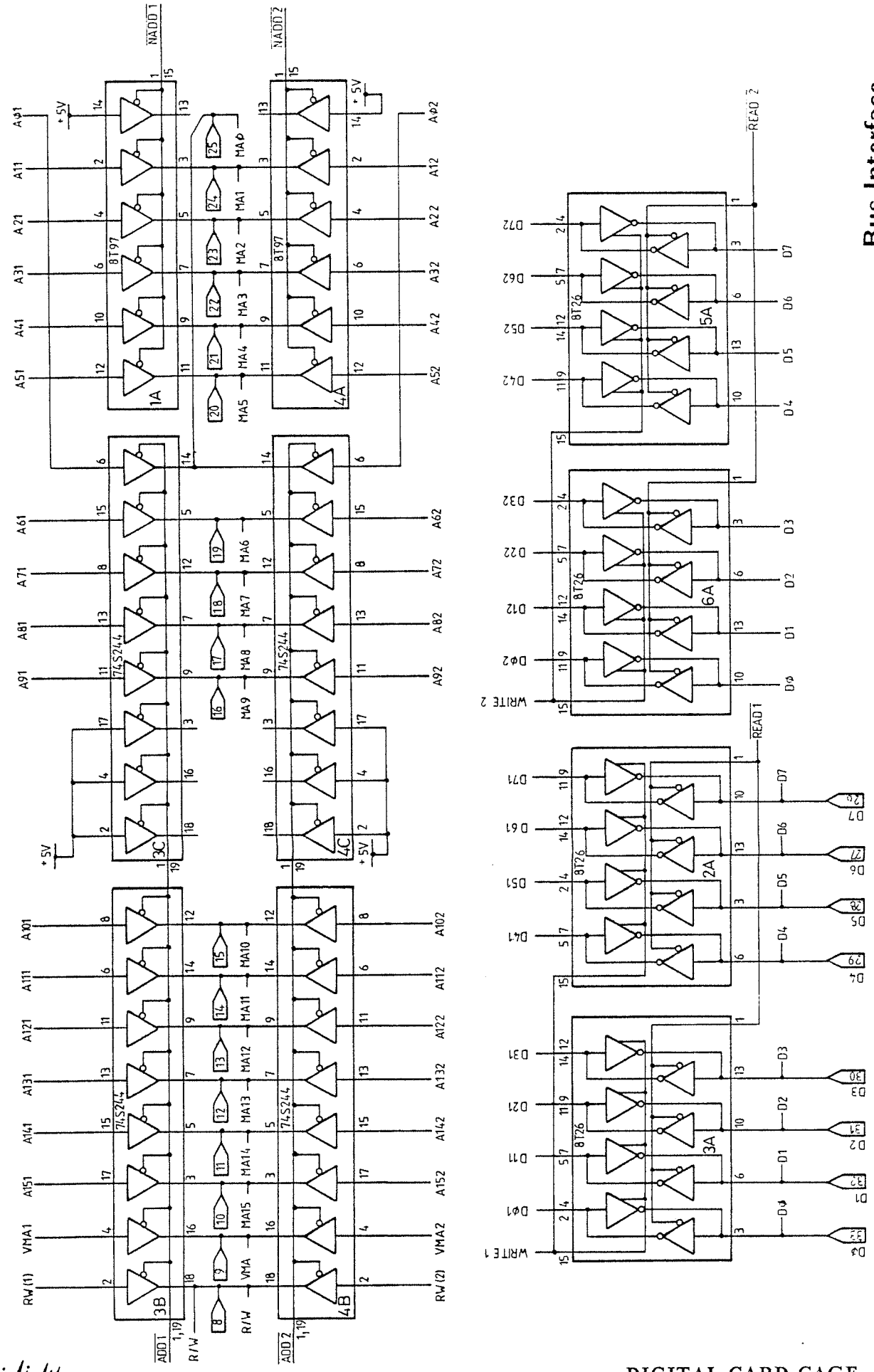
Option	CPU	LINK	Function
W1	P1	1-2 *	enable map select output
		2-3	disable
W2	P1	1-2 *	enable DMA to select A map
		2-3	disable
W3	P2	1-2 *	enable map select output
		2-3	disable
W4	P2	1-2 *	enable DMA to select A map
		2-3	disable
W5	P1	1-2	disable P1 DMA during indivisible P2 cycles
		2-3 *	enable
W6	P2	1-2 *	disable P2 DMA during indivisible P1 cycles
		2-3	enable

These links are set by PCB traces in the positions marked by * . Links


Clock and Timing Generation,
DMA Control
DRAWN: PV REVISION: 7


Processors etc.
DRAWN: PV REVISION: 7
5,6B,C
1,2B,C
6809 E
74LS32
74LS04
74LS08
74LS00
74LS139
74LS259
74LS74
74LS86
74LS10
74LS05
7402
74LS02
IRQ2
FIRQ2
HALT
NMI
IRQ
FIRQ
R/W
RESET
BUSY
VCC
VSS
TSC
LIC
BA
BS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
RES 1
RES 2
SYRES
RDMEN
VMA1
VMA2
HANG 1
HANG 2
VFETCH 1
VFETCH 2
INT(1)
INT(2)
ADD1
ADD2
BA1
BA2
R1
3K3
+5V


Map Switching. Interrupt Control
DRAWN: PV REVISION: 7
8T26
7C
8C
9C
9B
8B
9A
8A
7A
7B
74LS00
74LS04
74LS08
74LS32
74LS10
74LS13
74LS14
74LS138
74LS273
74LS74
74LS191
74S374
7427
7E
7D
F3
W1
W2
W3
W4
+5V
AB1
AB2
D0
D1
D2
D3
BD0
BD1
BD2
BD3
MS1
MS2
DMA1
DMA2
CPU1E
CPU2E
ILS1
ILS2
ILC1
ILC2
INT1
INT2
RA1
P1LS
P2LS
SET
SYRES
VFETCH 1
VFETCH 2
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA0
MAS
ADD(1)
ADD1
ADD2
R/W
FCXX
IA11
IA21
IA31
IA41
IA12
IA22
IA32
IA42


Bus Interface
DRAWN: PV REVISION: 7
NADD 1
NADD 2
ADD 1
ADD 2
R/W
READ 1
READ 2
WRITE 1
WRITE 2
74S244
8T97
8T26
1A
2A
3A
4A
5A
6A
3B
4B
3C
4C
+5V
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
VMA
VMA1
VMA2
RW(1)
RW(2)