Internal Logic Circuits

• Reset

The sequencer circuit of this product is initialized after logic supply (V_{DD}) is applied, and the power on reset function operates. To initialize the sequencer, the output immediately after power-on indicates that the status that the power circuits are in the home state. In a case where the sequencer must be reset after motor has been operating, a reset signal must be inputted on the RESET pin. In a case in which external reset control is not necessary, the RESET pin is not used, and must be fixed at a logic low level on the application circuit board.

• CLOCK Input

When the CLOCK input signal stops, excitation changes to the motor Hold state. At this time, there is no difference if the CLOCK input signal is at the low level or the high level. The SLA7070M series is designed to move 1 step at a time, when a Clock pulse edge is detected.

• Chopping Synchronous Circuit

The SLA7070M series has a chopping synchronous function to protect from abnormal noises that may occasionally occur during the motor-Hold state. This function can be operated by setting the SYNC terminal at high level. However, if this function is used during motor rotation, control current does not stabilize, and therefore this may cause reduction of motor torque or increased vibration. So, Sanken does not recommend using this function while the motor is rotating. In addition, the synchronous circuit should be disabled in order to control motor current properly in case it is used other than in dual excitation state (Modes 8 and F) or single excitation Hold state.

In normal operation, generally the input signal for switching can be sent from an external microcomputer. However, in applications where the input signal cannot be transmitted adequately due to limitations of the port, the following method can be taken to use the functions.

The schematic diagram in figure 8 shows how the IC is designed so that the Sync signal can be determined by the CLOCK input signal. When a logic high signal is received on the CLOCK pin, the internal capacitor, C, is charged, and the Sync signal is set to logic low level. However, if the Clock signal cannot rise above logic low level (such as when the circuit between the microcomputer and the IC is not adequate), the capacitor is discharged by the internal resistor, R, and the Sync signal is set to logic high, causing the IC to shift to synchronous mode.

The RC time constant in the circuit should be determined by the minimum clock frequency used. In the case of a sequence that keeps the CLOCK input signal at logic high, an inverter circuit must be added. In a case where the Clock signal is set at an undetermined level, an edge detection circuit (figure 9) can be used to prepare the signal for the CLOCK input, allowing correct processing by the circuit shown in figure 8.

• Output Disable (Sleep1 and Sleep2) Circuits

There are two methods to set this IC at motor free-state (coast, with outputs disabled). One is to set the REF/SLEEP1 pin to more than 2 V (Sleep1), and the other (Sleep2) is to set the excitation signals (pins M1, M2, and M3). In either way, the IC will change to Sleep mode, stopping the main power supply at the same time, and decreasing circuit current. The difference between the two methods is that, in the first way, the internal sequencer remains in an enabled state, and in the latter method, the IC enters the Hold state. Moreover, in the method using

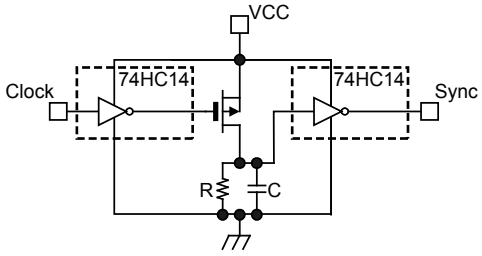

Figure 8. Clock signal shutoff detection circuit, using 74HC14s.

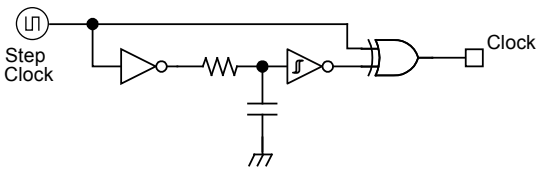

Figure 9. Clock signal edge detection circuit, inputs to example circuit shown in figure 8.